SECTION 4 THEORY OF OPERATION

4.1 GENERAL.

4.2 This section covers the theory of operation of the Series 8000B Counter. Operation of the unit is dependent on the measurement mode selected. For this reason, general operating principles of each mode of operation are described first followed by individual circuit descriptions. Where circuitry differences occur between models, the models covered are identified.

4.3 Drawings in this section are included for explanation only. For specific reference designators, wiring details, etc., refer to the complete schematics in Section 6.

4.4 MEASUREMENT MODES.

4.5 Figures 4.2 through 4.11 summarize the basic principles of each operating mode in simplified form. Any point (positive or negative) on the input waveform can be selected to trigger the generation of pulses to the main gate.

4.6 The block labeled "counter" refers to both a high-speed decade on the Switch board and the display counter. The high-speed decade divides its input by 10 and advances the display counter. It also updates the least-significant readout position (figure 4.1).

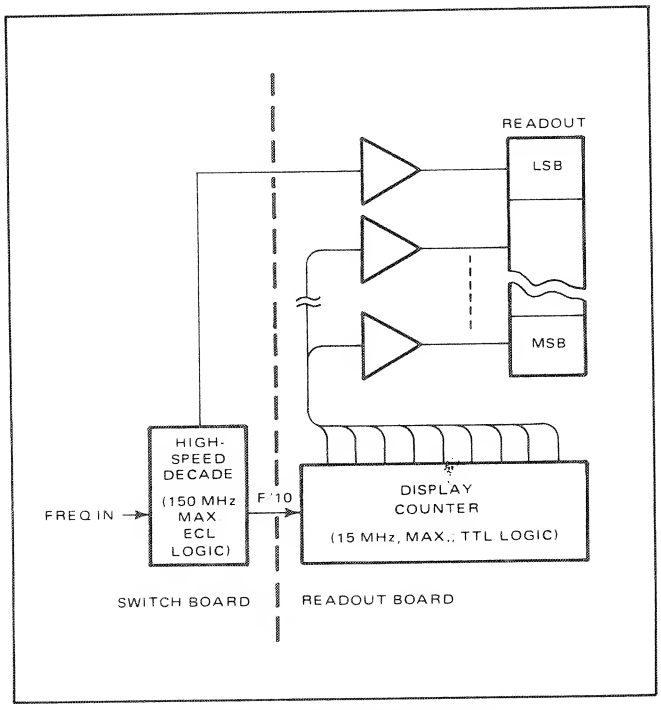

Figure 4.1 - Counter Definition

4.7 The "Display" block includes quad-latches and drivers for each of the readout positions (bits), and the readout tubes.

4.8 The "Reference Frequency" block can be either an external reference frequency or the internally generated reference frequency. The internal reference includes the reference oscillator (on Readout board), and the reference conditioning circuits (on the Switch board).

4.9 "Main Gate" refers to the logic that generates the signal $\overline{\Delta t}$. This signal controls the times at which the counter begins or stops counting. Counter operation is dependent on the mode of operation and other selections made by the operation (timebase, input trigger level, etc).

4.10 Self-Check Mode.

4.11 The Self-Check mode of operation (figure 4.2) enables the operator to check for proper operation of the counter. The reference frequency is used for two purposes. It is counted by the counter during the measurement time and it generates the time base frequency that produces the gating signal. Proper operation of the counter is determined by varying the time base and observing the readout (see Section 3, table 3.3).

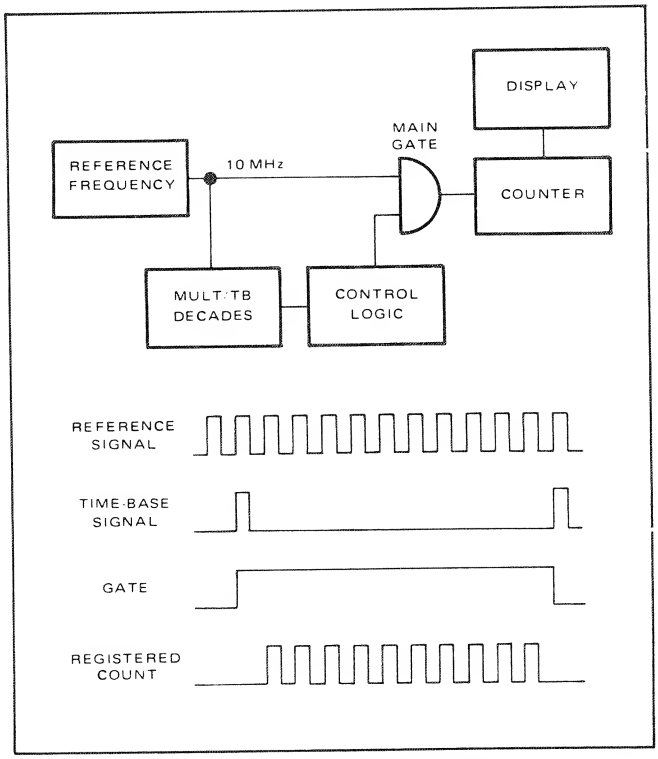

Figure 4.2 - Self-Check Mode

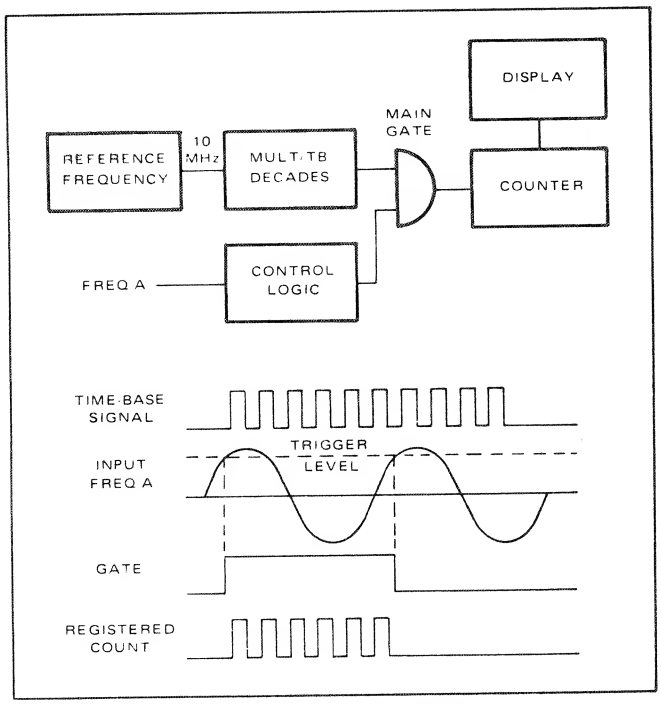

Figure 4.3 - Period Mode

4.12 Period Mode.

4.13 Period is the inverse of frequency. Therefore, frequency A is applied to the control logic and the reference frequency is connected to the multiplier/timebase decades (figure 4.3).

4.14 Clock pulses are derived by dividing down the 10 MHz reference oscillator output. The specific decade division is determined by the setting of the MULTIPLIER/ TIMEBASE switches. The output of the M/TB decades is presented to the input of the counter. Trigger pulses resulting from two consecutive signals from input A are applied to the control logic. The first trigger pulse opens the main gate; the next pulse closes it. During "gate open" time, the counter counts the applied clock pulses. The count is displayed on the readout directly in microseconds, milliseconds, or seconds, according to the MULTIPLIER/ TIMEBASE switch setting.

NOTE

Low Frequencies may be determined more accurately by measuring period rather than frequency directly. This is because the longer period of a low frequency allows more counts to accumulate in a period measurement. Therefore, resolution and accuracy are both improved.

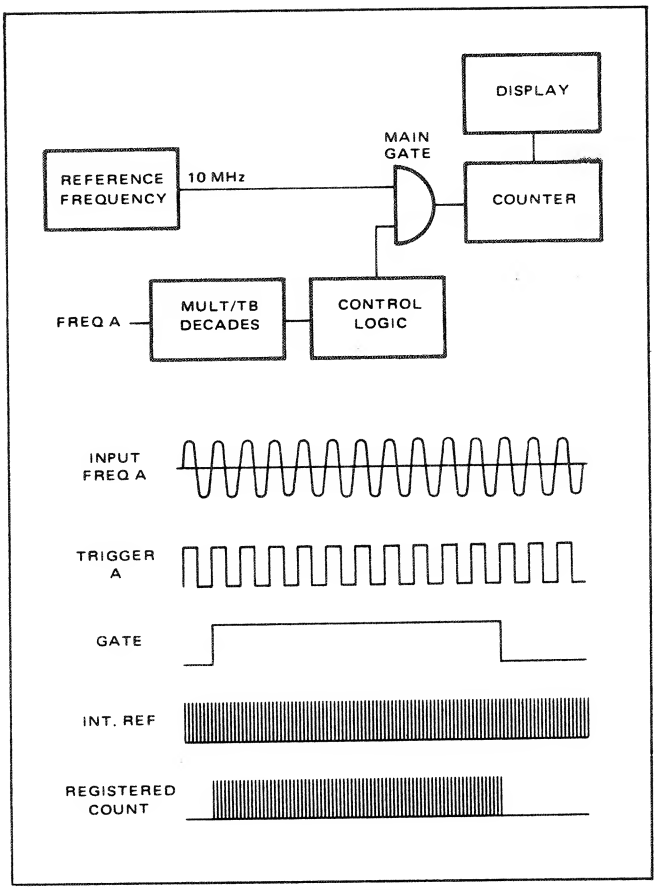

Figure 4.4 - Period Average Mode

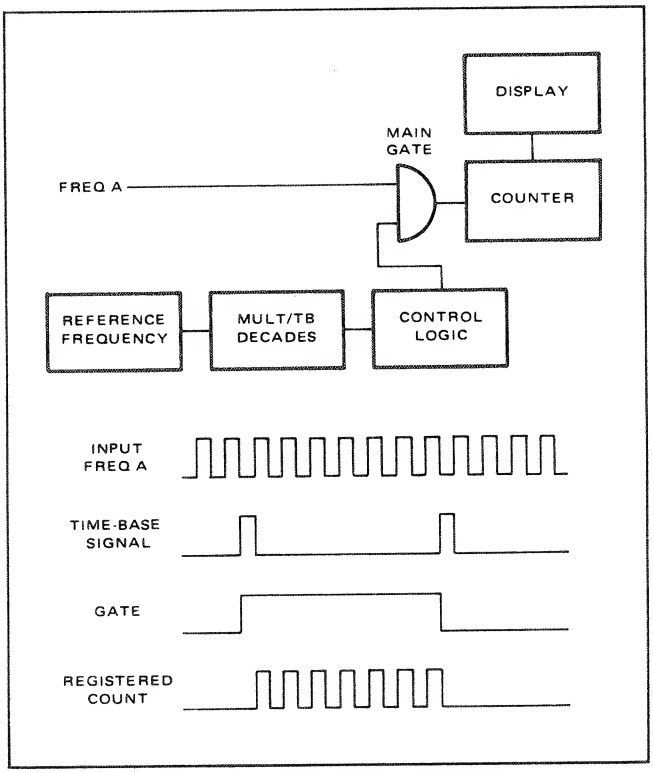

Figure 4.5 - Frequency "A" Mode

4.15 Period Average Mode.

4.16 Period Average mode is used to obtain increased resolution and accuracy over period measurements. The more periods over which a signal is averaged, the greater the accuracy of the measurement.

4.17 In this mode of operation (figure 4.4), the reference oscillator is routed directly to the main gate and the unknown frequency is routed through the multiplier/time base decades to the control logic which, in turn, controls the main gate. The pulses occurring during main "gate open" are counted, stored, and an accurate readout measurement is displayed. The "gate open" period is determined by the setting of the MULTIPLIER/TIMEBASE switches.

4.18 Frequency A Mode.

4.19 During direct frequency measurements, the counter compares the unknown frequency against the known reference frequency (figure 4.5).

4.20 Input signal F_a is routed to the main gate of the counter. The internal reference supplies a 10 MHz signal through the multiplier/time base decades and through the control logic to control the main gate.

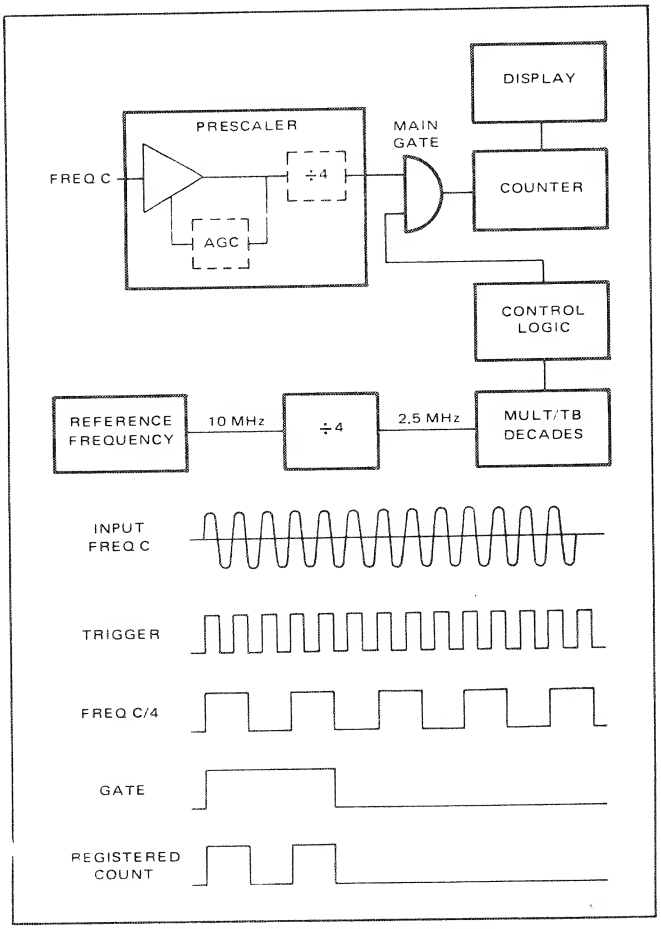

Figure 4.6 - Frequency C Mode

4.21 The number of input pulses accumulated during the main "gate open" interval is a measurement of the input frequency. The count obtained is displayed on the readout. This display may be retained until such a time as a new sample is ready to be displayed.

4.22 Frequency C Mode. (Not available in Model 8010B.)

4.23 In the Frequency C mode, the unknown frequency is applied to the main gate through the prescaler. The prescaler includes an amplifier, automatic gain control circuit, and a divide-by-four circuit (figure 4.6).

4.24 The AGC circuit maintains the required amplifier gain which alleviates the need for manual trigger and range control. The divide-by-four circuit is necessary to reduce the unknown frequency to a frequency which the main counter circuitry can count. The reference frequency is also divided by four to enable direct readout. The actual gate time is four times the selected time base.

4.25 Totalize Mode.

4.26 In Totalize mode, the main gate is controlled by the manual START/STOP switch on the front panel of the instrument or external START/STOP commands (figure 4.7).

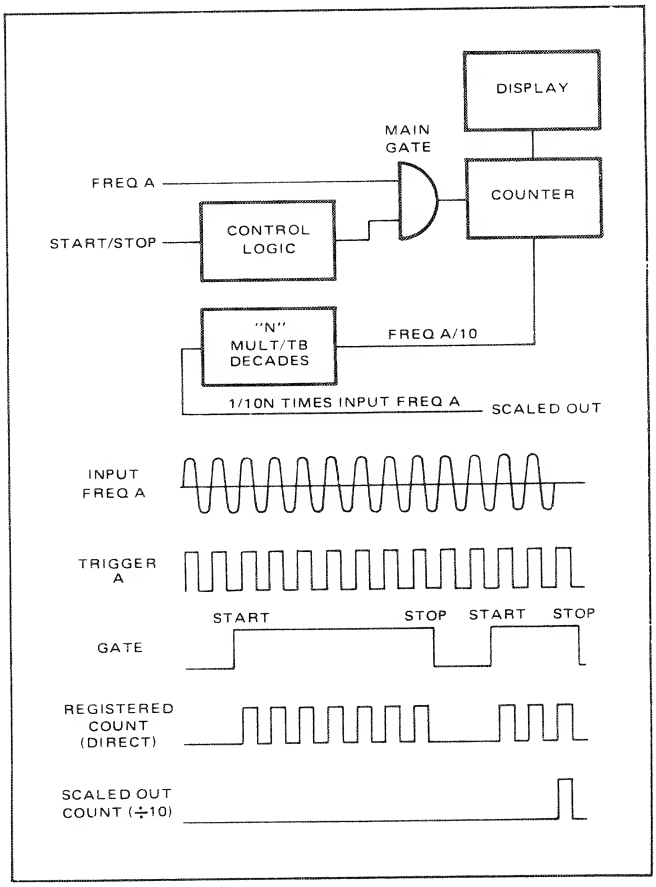

Figure 4.7 - Totalize Mode

4.27 With the first Start/Stop command, the control logic opens the main gate allowing the input pulses to be totalized by the counter. Simultaneously, a continuous update is supplied to the flip-flops which make up the display latches. The counter readout then represents the input pulses received during the interval between "start" and "stop". External start/stop commands may be applied via the REMOTE connector if equipped with the systems interface option.

4.28 In this mode, the instrument delivers a scaled output frequency to a connector on the rear panel, SCALED OUT. The output is the input signal frequency scaled by 1/10N where N is the multiplier setting.

4.29 Time Interval Mode.

4.30 The Time Interval mode of operation allows measurement of the time between two electrical events to a maximum resolution of 100 nanoseconds (figure 4.8). The first event (start) is connected to channel A and opens the gate. The second event (stop) is connected to channel B and closes the gate. These signals control the main gate through the control logic. Slope and trigger level controls on the front panel allow variable trigger levels on the + or – slope of the input waveforms. Pulses from the 10 MHz reference oscillator are routed to the multiplier/timebase decades and to the main gate.

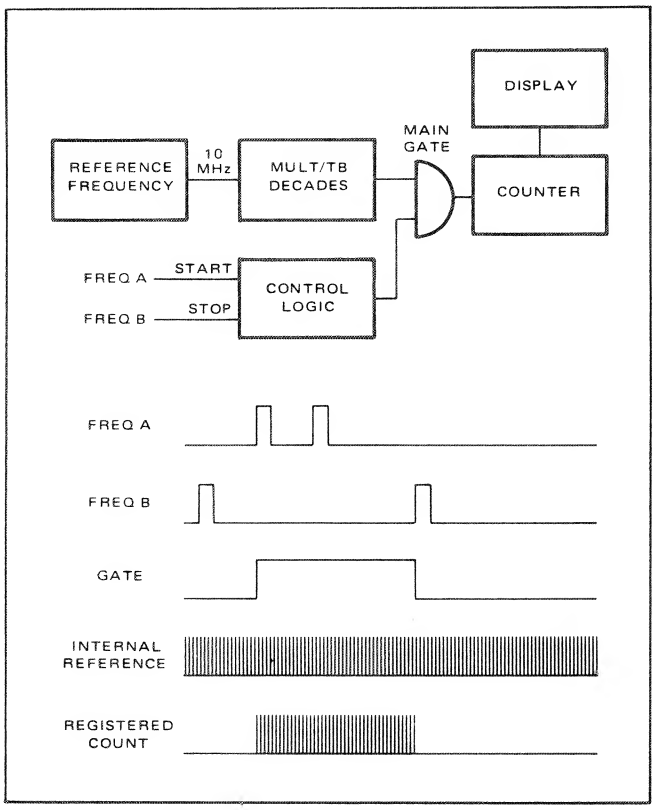

Figure 4.8 - Time Interval Mode

4.31 The pulses occurring during the main gate are counted and displayed. Channel A can be triggered after the channel B trigger in 30 ms on a single time interval measurement.

4.32 Time Interval Average.

4.33 Similar to the Time Interval mode of operation, the Time Interval Average mode measures the count accumulated during a multiple of intervals (figure 4.9). It then averages the count by shifting the decimal point and displaying the result. This mode of operation makes it possible to achieve greater resolution and accuracy when measuring time intervals. The A trigger point can follow the B trigger point as close as 200 nanoseconds.

> **NOTE**
>
> In T.I. Average mode, the input signals must be repetitive and asynchronous with the counter's time base.

4.34 A/B (Ratio) Mode.

4.35 This mode is identical in function to the frequency measurement modes, but substitutes an external signal for the reference frequency (figure 4.10).

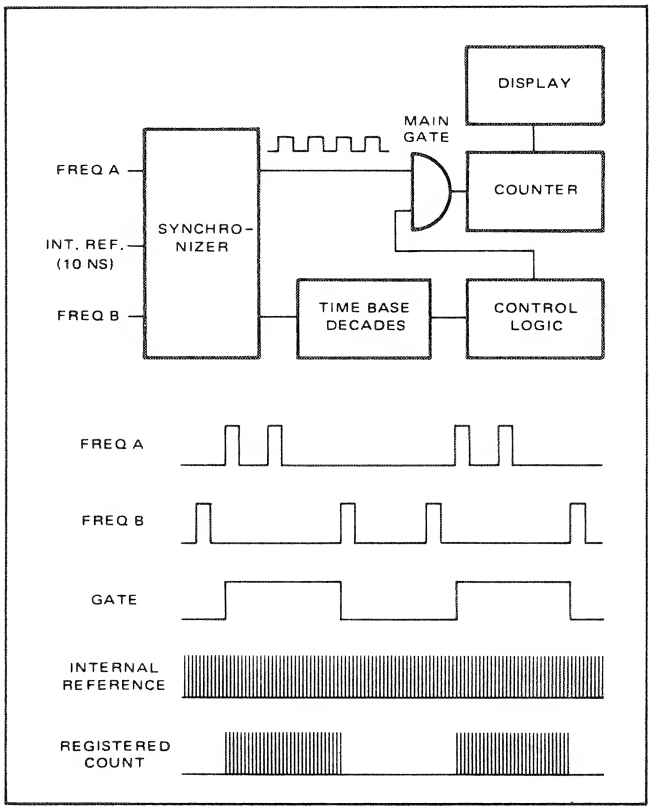

Figure 4.9 - Time Interval Average Mode

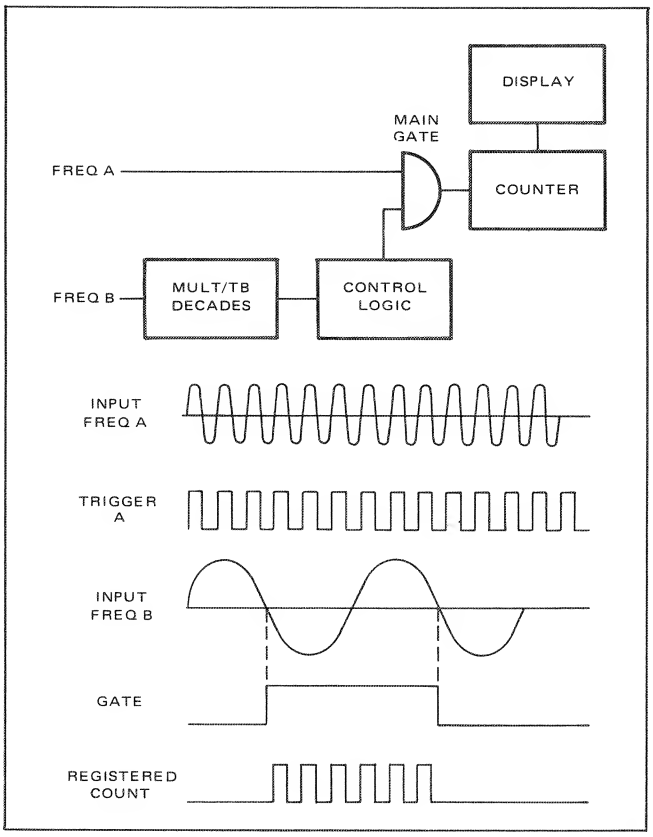

Figure 4.10 - A/B Ratio Mode

4.36 The higher of the two frequencies which are to be measured is connected to input A; the lower frequency to input B. Input B is applied to the multiplier/timebase decades. The higher the multiplier/timebase selected, the greater the resolution and the longer the measurement time. Two successive trigger pulses derived from the multiplier/timebase decades applied to input B open and close the main gate. During the "gate open" interval, the counter counts the trigger pulses derived from input A and the ratio Fa/Fb is then displayed on the readout.

4.37 CIRCUIT DESCRIPTIONS.

4.38 A block diagram of the counter is shown in figure 4.11. The circuit descriptions to follow make reference to the schematics in Section 6 as well as to partial schematics within this section.

4.39 Prescaler (Schematic: figures 6.13 and 6.15). Not available in Model 8010B.

4.40 The Prescaler provides the signal conditioning function for channel C. It accepts frequencies from 1 MHz to 550 MHz (10 MHz to 500 MHz with 030 option), automatically controls the amplitude of the signal, and divides the frequency of the signal by a factor of four. The scaling reduces the incoming signal to a rate compatible with the

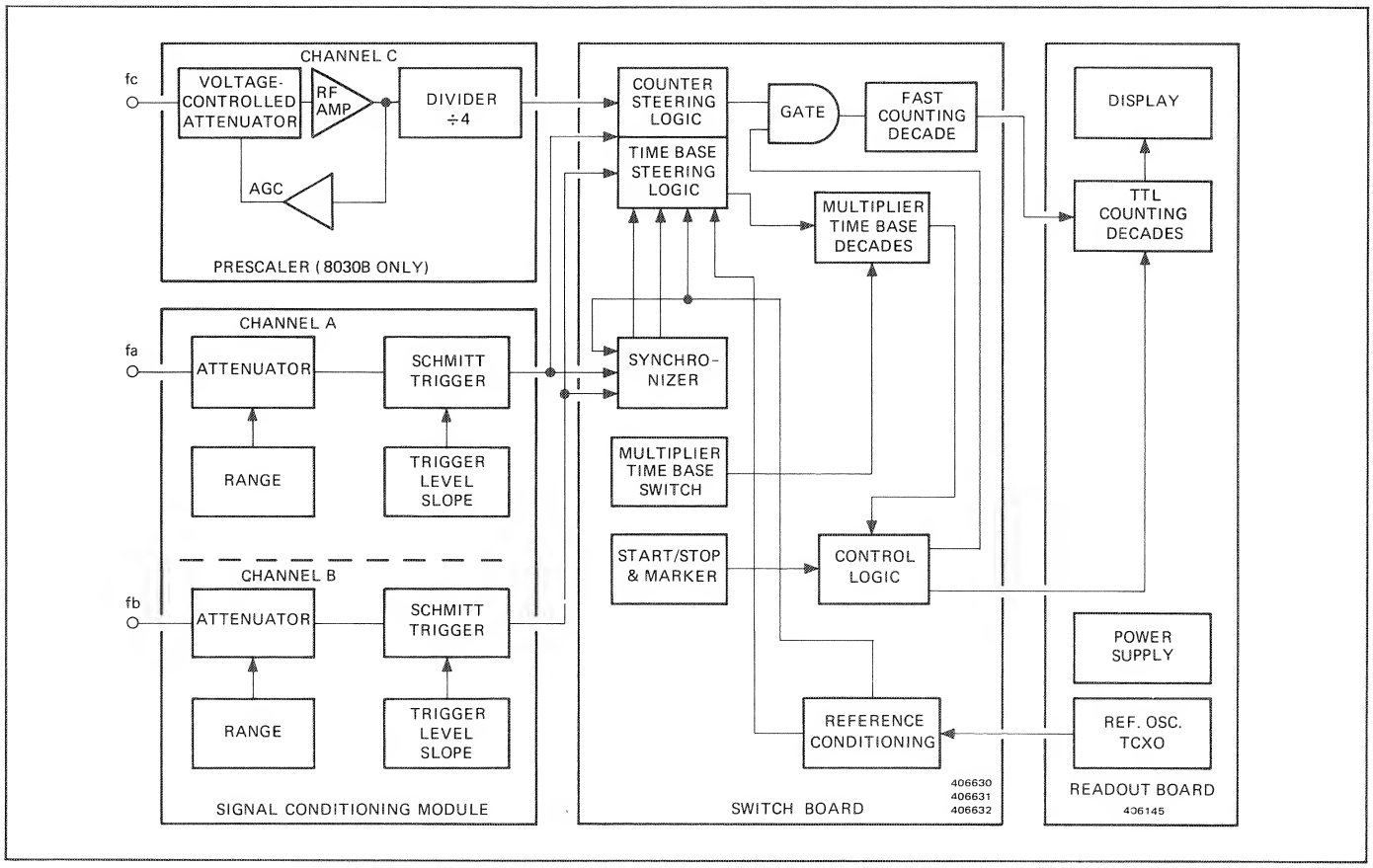

Figure 4.11 - Functional Block Diagram (All Models)

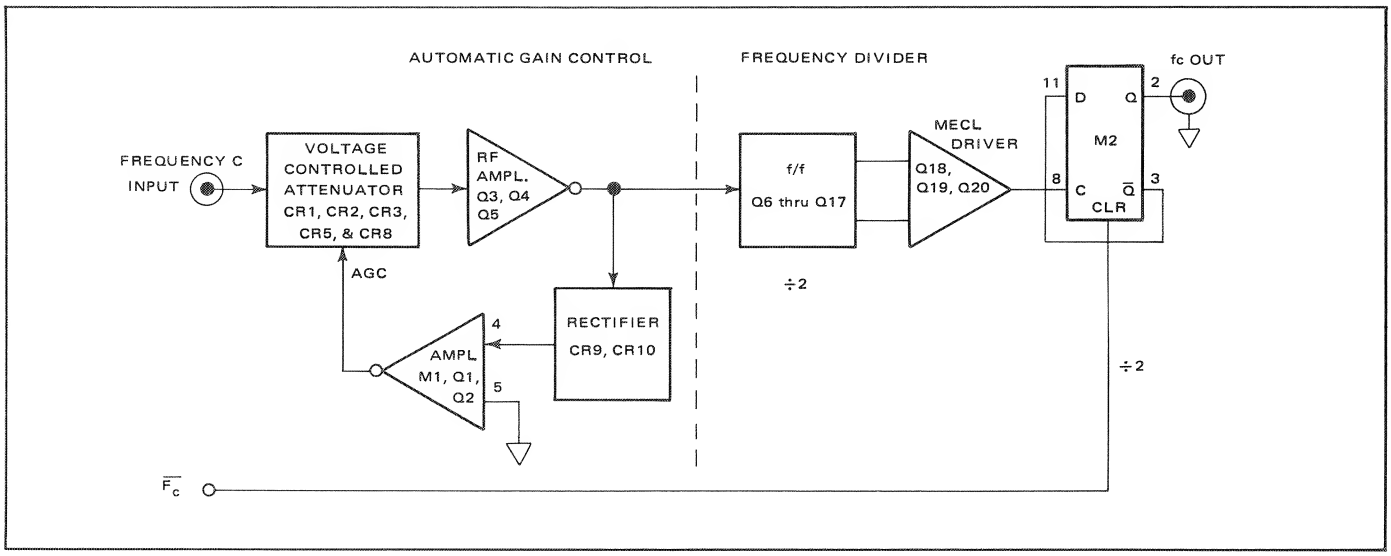

Figure 4.12 - 550 MHz Prescaler

high-speed decades. The circuitry, shown simplified in figure 4.12, is divided into two sections: the automatic gain control section (including the attenuator) and the frequency divider section.

4.41 AUTOMATIC GAIN CONTROL.

4.42 The "C" input signal from the input connector passes through the voltage-controlled attenuator to the RF amplifier. The attenuator consists of two diodes in series with the signal path and three diodes shunting the signal path. With no signal from the AGC amplifier (M1), series diodes CR2 and CR5 are forward-biased providing a low impedance signal path while shunting diodes CR1, CR3, and CR8 are back-biased and provide little attenuation to the signal. As the AGC signal goes negative, series diodes CR2 and CR5 conduct less, increasing their apparent impedance while the diodes in shunt begin conducting and attenuating the signal. The signal from the attenuator passes through the three-stage amplifier (Q3, Q4, and Q5) which increases the signal level to approximately 200 mV rms. The AGC circuit maintains 200 mV rms at the bases of Q11 and Q14.

4.43 The output of the amplifier is applied to the divider section and to a voltage rectifier circuit consisting of diodes CR9 and CR10. The rectifier produces a positive dc voltage level proportional to the RF level of the amplifier output which, after amplification and inversion by differential amplifier M1, controls the attenuator. The gain control circuit holds the signal level of the amplifier input to approximately 50 mV (1 mV with option 030). With option 030, operation is the same as described for the standard Prescaler, but an additional stage of amplification is included (see schematic, figure 6.15).

4.44 FREQUENCY DIVIDER.

4.45 This portion of the Prescaler consists of a discrete transistor flip-flop, a driver circuit (Q18, Q19, and Q20), and a ECL* type D flip-flop, M2. The discrete transistor flip-flop consists of transistors Q6 through Q17. The function of this circuit is to divide the frequency of the signal by two. At low frequency operation, the information is transferred so fast (on the positive edge of the pulse) that it is possible for the flip-flop to go into oscillation at a natural resonate frequency of 300 MHz. A Skew circuit is employed to guard against self oscillation.

4.46 The driver stage for the discrete flip-flop consists of Q8, Q11, Q14, and Q17. The level at which transistors Q8 and Q11 switch is the same at all frequencies. The level at which transistors Q14 and Q17 switch is controlled by the skew circuit consisting of C35, CR16, R55, R59, and C38. The output of the skew circuit is frequency dependent. At frequencies below 300 MHz, the current path is from −18V through resistors R59, R55, and diode CR16 to ground. This biases Q17 at −.2V. Below 300 MHz, the input signal has to overcome the −.2V bias on Q17 base before the flip-flop toggles. As the frequency goes above 300 MHz, the impedance of capacitor C35 decreases and the signal coupled by C35 increases in amplitude. The signal is rectified by CR16. As the frequency continues to increase, capacitor C38 charges to a higher DC level (approaching zero) removing the −.2 volts bias.

4.47 Diodes CR11 through CR14 are level shifters which increase the rise and fall time of the discrete flip-flop. The output of the discrete flip-flop is amplified by Q18, Q19,

*emitter-coupled logic

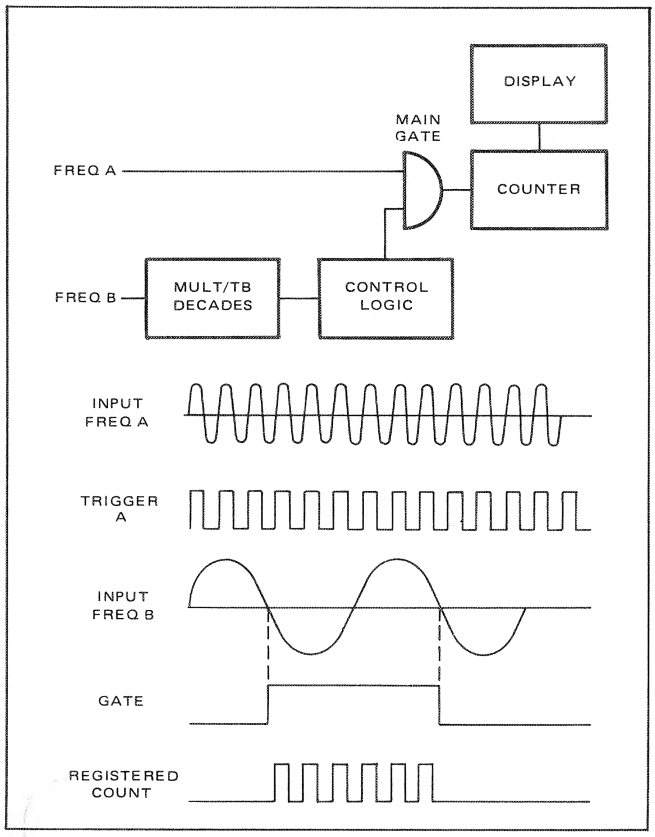

Figure 4.10 - A/B Ratio Mode

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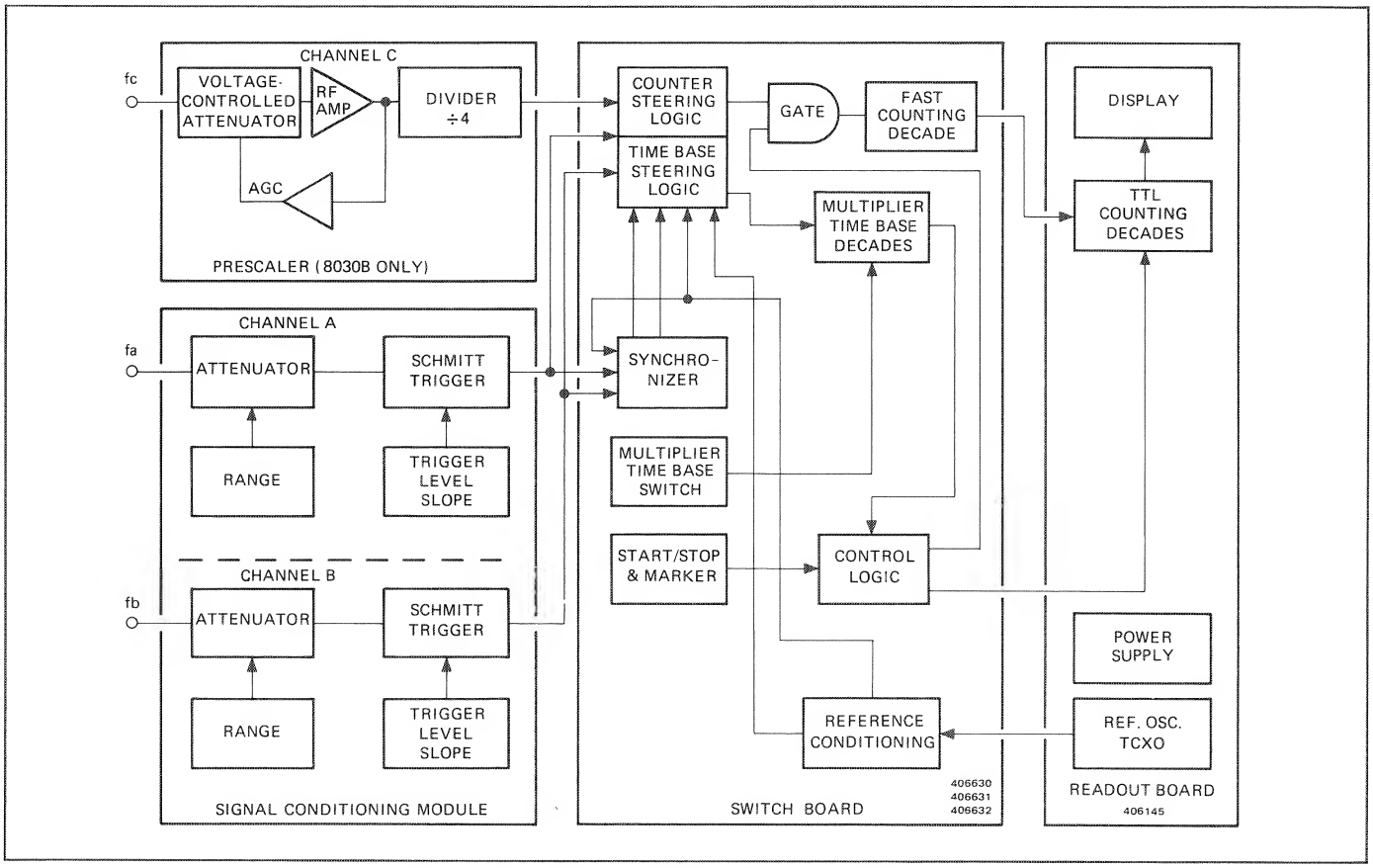

Figure 4.11 - Functional Block Diagram (All Models)

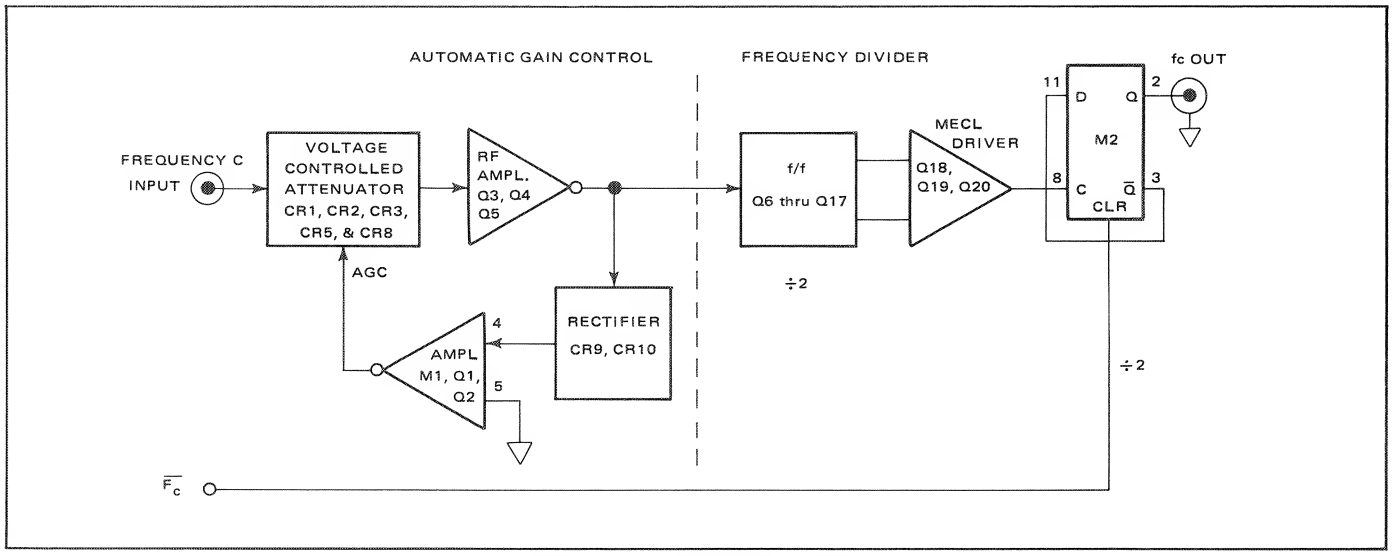

Figure 4.12 - 550 MHz Prescaler

high-speed decades. The circuitry, shown simplified in figure 4.12, is divided into two sections: the automatic gain control section (including the attenuator) and the frequency divider section.

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4.43 The output of the amplifier is applied to the divider section and to a voltage rectifier circuit consisting of diodes CR9 and CR10. The rectifier produces a positive dc voltage level proportional to the RF level of the amplifier output which, after amplification and inversion by differential amplifier M1, controls the attenuator. The gain control circuit holds the signal level of the amplifier input to approximately 50 mV (1 mV with option 030). With option 030, operation is the same as described for the standard Prescaler, but an additional stage of amplification is included (see schematic, figure 6.15).

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4.47 Diodes CR11 through CR14 are level shifters which increase the rise and fall time of the discrete flip-flop. The output of the discrete flip-flop is amplified by Q18, Q19,

*emitter-coupled logic

and Q20. The signal is applied to ECL flip-flop M2. The reset line of M2 is controlled by $\overline{Fc}$. When Frequency C is selected $\overline{Fc}$ is false, M2 is released from the reset state and divides the frequency of the signal by two. The signal (now divided by four) is fed to the input gate of the steering logic. When $\overline{Fc}$ is true, Frequency C is not selected and the flip-flop M2 output is held in the reset state.

4.48 Signal Conditioning Module (Schematic: figure 6.2).

4.49 In Model 8020B, the Signal Conditioning Module conditions the signal to be compatible with ECL logic and establishes the trigger level of the channel A input. In Models 8010B and 8030B, an additional (and basically identical) module is used for conditioning the channel B input.

4.50 In dual-channel models, the input to the channel B Signal Conditioning Module comes from either of two sources depending on the position of the SEP/COM switch. In the COM (common) position, the B input signal is from the channel A input connector (and common with A). In SEP (separate), the signal is from the B input connector (figure 4.13).

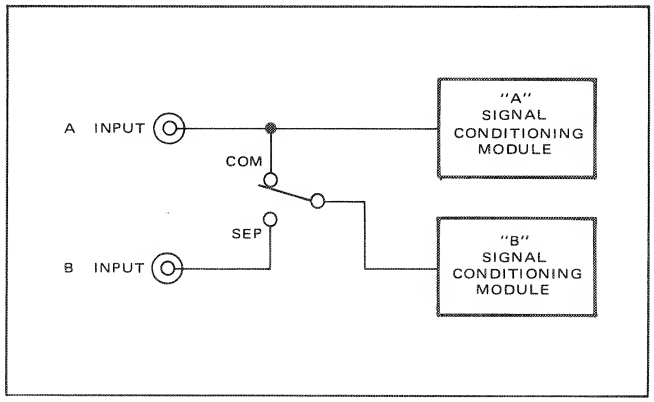


Figure 4.13 - SEP/COM Switch

4.51 Since the modules are identical for channels A and B, only channel A Signal Conditioning is described.

4.52 CHANNEL A ATTENUATOR (figure 4.14).

4.53 With the AC/DC coupling switch set to AC, the signal applied to input A flows through capacitor C1; with DC selected, the capacitor is bypassed through the coupling switch, S207. The signal flows through the attenuator according to the range selected. In the 1-volt range, the signal passes directly through the INPUT VOLTAGE range switch; in the 10-volt range, the signal is attenuated by a factor of 10 (20 dB); and in the 100 volt range, the signal is attenuated by a factor of 100 (40 dB). From the range switch, the signal passes through 100-kilohm resistor R4 in parallel with 47 pfd capacitor C2 to the signal conditioning network.

4.54 SCHMITT TRIGGER.

4.55 As shown in figure 4.14, the signal from the channel A attenuator (f_a in) flows through emitter follower circuits Q1 and Q2. Transistors Q4 and Q8 form a gain stage to drive the input side of a Schmitt trigger consisting of transistors Q3, Q5, Q6, and Q7. The signal from the attenuator is prevented from exceeding ±4 volts by clamp zener diodes CR1, CR2 and diodes CR3 and CR4. The trigger level of the trigger circuit is determined by the potential applied to the input of the follower circuits consisting of Q9 and Q10. With PRESET selected (the extreme counter-clockwise position of the front panel trigger level

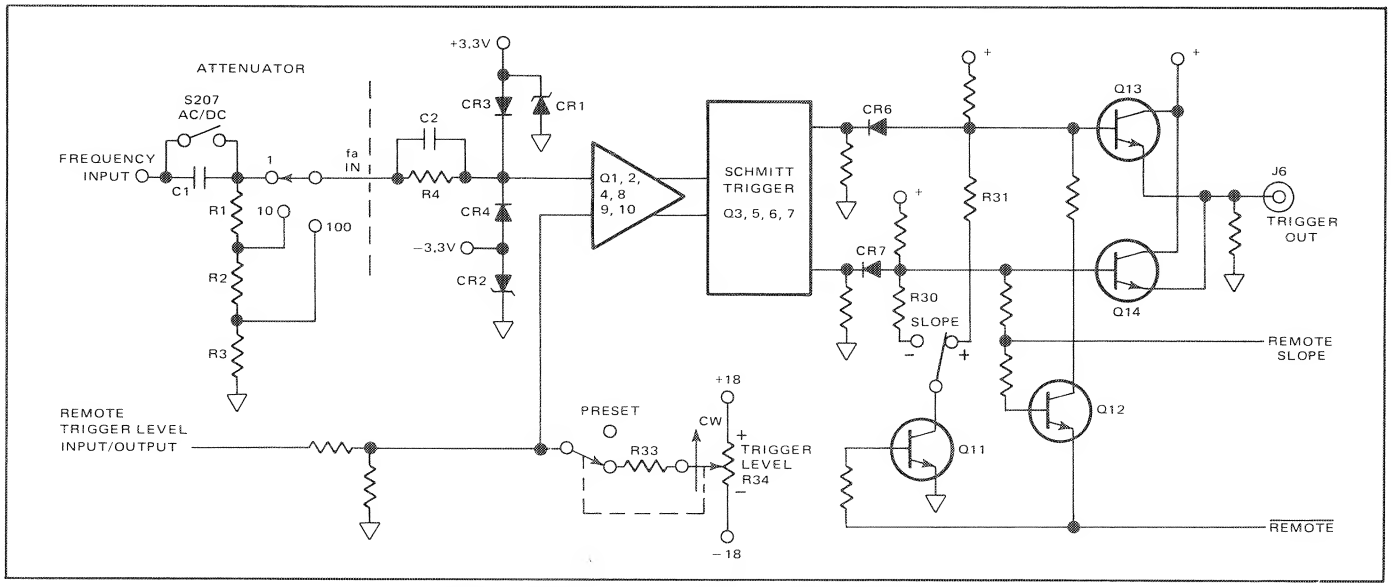


Figure 4.14 - Signal Conditioning Block Diagram

control) and assuming no remote level input, the trigger level is approximately zero volts (0 VDC ± 5% of the input voltage range selected). With PRESET out, the trigger level is adjustable by the trigger level control across ±300% of the range selected. The trigger level may be monitored by connecting a voltmeter across the analog output on the rear panel.

4.56 SLOPE.

4.57 The trigger circuit generates two outputs (180° out of phase) which are gated through diode CR6 or diode CR7, depending on the position of the +/– slope switch. With + slope selected, the anode of diode CR6 is held low through R31 and Q11. A positive pulse is generated during the positive-going edge of the input signal and passes through CR7, through Q14 to connector J6. With – slope selected, the anode of diode CR7 is held low through R30 and Q11. A positive pulse, generated during the negative-going edge of the input signal, passes through CR6 through Q13 to connector J6. When Remote is not selected, transistor Q11 is conducting and the signal that appears at J6 is determined by the position of the +/– (slope) switch on the front panel. In Remote, Q11 is off and Q12 determines the signal at J6.

4.58 Switch Board Assembly (Schematic: figure 6.4).

4.59 The Switch board assembly is one of two large printed circuit boards mounted to the base plate. The Switch board is accessible from the bottom of the counter. The switch board contains the following circuits: time base decades and switches, counter and time base steering logic, fast counting decade, control logic, reference conditioning, and a synchronizer circuit. Each circuit is described in the following paragraphs.

4.60 REFERENCE CONDITIONING CIRCUIT.

4.61 The Reference Conditioning circuitry converts the reference signal to a 10 MHz square wave and routes it to the steering circuits. This circuit processes a reference signal supplied either from the internal frequency source or from an external frequency standard through rear panel connector J106. The source is selected by the rear panel REF switch S102. The internal frequency source is a self-contained, temperature-compensated oscillator located on the Readout board. The external reference (1, 5, or 10 MHz) must be capable of delivering 1 volt RMS at connector J106 (input impedance is 1K ohm). With the REF switch set to the EXT position, an external signal is fed to the input of the conditioning circuitry and the signal path from the internal frequency source is open; with the INT position selected, the internal frequency source is supplied to the input of the conditioning circuitry and the output of the conditioning circuitry is routed to connector J106 for use as a secondary standard source.

4.62 The circuit is shown in simplified form in figure 4.15. The signal from the REF switch is shaped by the limiting action of inverter MA2 and applied to the Schmitt trigger circuit consisting of two inverters (MA2). The output is a square wave. The trigger output is differentiated through a capacitor-resistor combination (C37, R98) and the negative spikes from the differentiated signal are applied to the crystal filter circuitry (Q19, Y1). This circuit produces a 10 MHz damped oscillation that is sustained by input spikes at 10 MHz or by subharmonics at 1 and 5 MHz. The

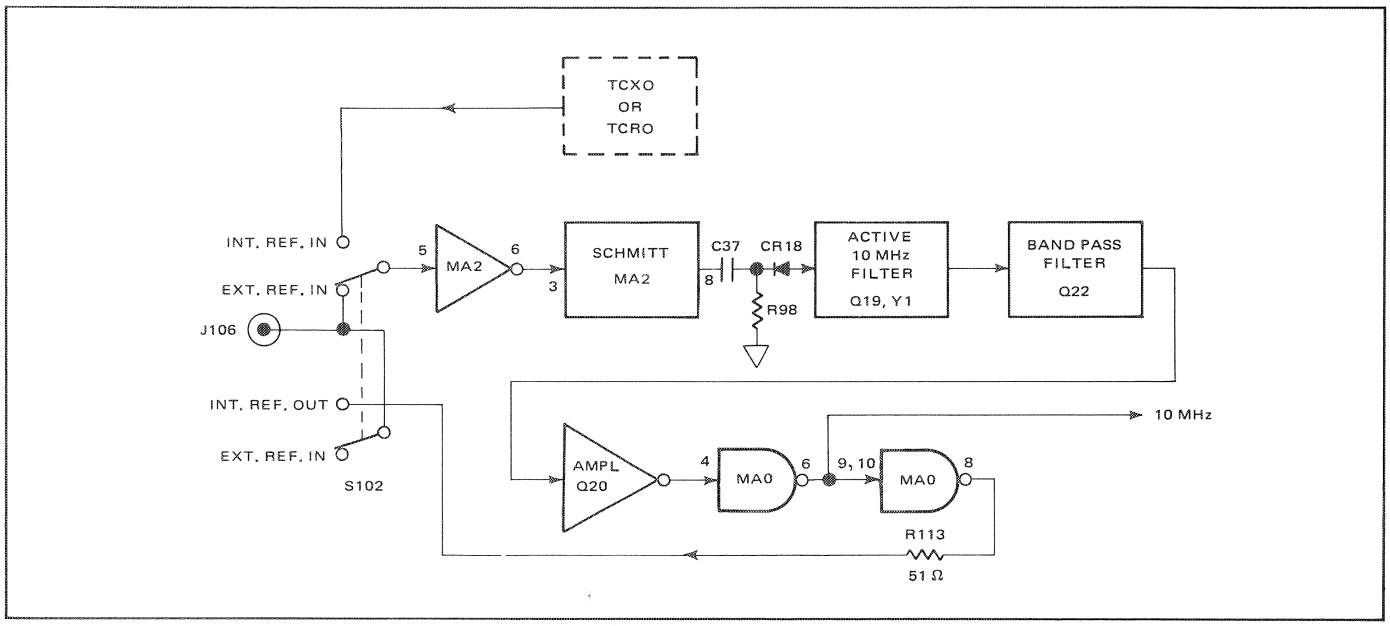


Figure 4.15 - Reference Conditioning Circuit

active filter output is applied to the bandpass filter, increasing the amplitude of the signal and removing the harmonics. The signal then flows through amplifiers Q20, Q21 and four NAND gates (MA0), two of which are used as inverters. The output of the first gate (MA0-6) is routed to the steering circuits in the instrument, the output of the second gate (MA0-8) passes through resistor R113 and the INT position of the reference switch to connector J106.

4.63 FAST COUNTING DECADE (Figure 6.4).

4.64 The Fast Counting Decade consists of four high-speed counters (MD2, MD3, and MD4) interconnected to form a divide-by-ten circuit. The BCD outputs of the counter are buffered and inverted through transistors Q3, Q4, Q5, and Q6 and routed to the quad latch ME9, driver MF9, and the least-significant digit readout of the Readout board. The buffered 4 and 8 bits from the decade are combined in NAND gate MC5 to form a quasi-square output (fa/10) with a frequency equal to 1/10 of the decade input signal. The counter is controlled by a gate signal applied to clock input C1 in the first flip-flop MD2. When C1 is false, the pulses at the clock input C2 are counted; when C1 is true, the flip-flop is inhibited. The gate control line connected to C1 is designated $\overline{\Delta t}$.

4.65 COUNTER STEERING LOGIC.

4.66 This circuitry routes signals to the input of the fast-counting decade according to the measurement mode selected. Signal flow through the circuit is shown in figure 4.16a through c.

4.67 Ratio, Totalize and Frequency A Modes (figure 4.16a).

4.68 Lines from the Ratio, Totalize and Frequency A positions of the FUNCTION switch are applied to a three-input NAND gate, MF5. The line for the selected mode is pulled low by the FUNCTION switch selection. The output of MF5 is high biasing CR1 and CR2 such that the f_a signal flows through CR1 and CR2 to MD1. MD1 is a ECL* four-input OR gate. The signal on pin 3 of MD1 causes the output of MD1 to change state (all other inputs to MD1 are low). The signal is routed to the clock input of MD2, a type D ECL flip-flop. Flip-flops MD2, MD3A, MD3B, and MD4 form a divide-by-ten fast-counting decade divider. The output of the fast counting decade drives the display counter on the Readout board and updates the least-significant digit of the readout.

4.69 Period and Time Interval Modes (figure 4.16b).

4.70 Signal flow in Period or Time Interval mode is as follows. Period or Time Interval is selected by the

*emitter-coupled logic

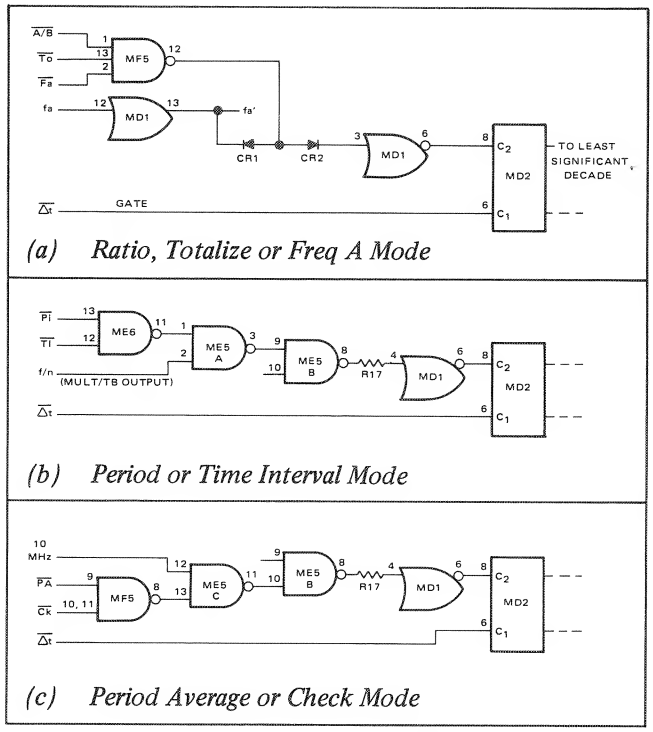


Figure 4.16 -Counter Steering Logic

FUNCTION switch, and one of the two lines, $\overline{PI}$ or $\overline{TI}$, is pulled to ground. These lines are connected to a two-input Nand gate, ME6. The output of ME6 goes high and is connected to the input to ME5A, a two-input Nand gate. The second input to ME5A is f/n. When the input line, pin 1, to ME5A is high, f/n is gated through ME5A and inverted. The signal is applied to the input (pin 9) of ME5B. The second input, pin 10, is high and the signal f/n is inverted through ME5B. The output of ME5B, f/n, goes to pin 4 of MD1, an ECL four-input NOR gate. The other three inputs to MD1 are low. The output of MD1 is routed to the clock input of the fast counting decade (MD2-8). The time that the counts are allowed to accumulate in the fast counting decade is controlled by $\overline{\Delta t}$ (main gate).

4.71 Period Average and Check (figure 4.16c).

4.72 Signal flow in Period Average or Check mode is as follows. Period Average or Check is selected by the FUNCTION switch, and one of the two lines, $\overline{PA}$ or $\overline{Ck}$, is pulled to ground. $\overline{PA}$ and $\overline{Ck}$ are connected to the inputs of a three-input Nand gate, MF5. The output of MF5 is high. The signal from MF5 is connected to two-input Nand gate, ME5C. The other input is connected to the 10 MHz Reference. The output of ME5C, (10 MHz) is connected to the input of a two-input Nand gate, ME5B. The other input to ME5B is high. The output of ME5B (10 MHz) is connected to the input of a four input ECL Nor gate, MD1. The other three inputs are low. The output of MD1 is routed to the clock input of the fast-counting decades (MD2-8).

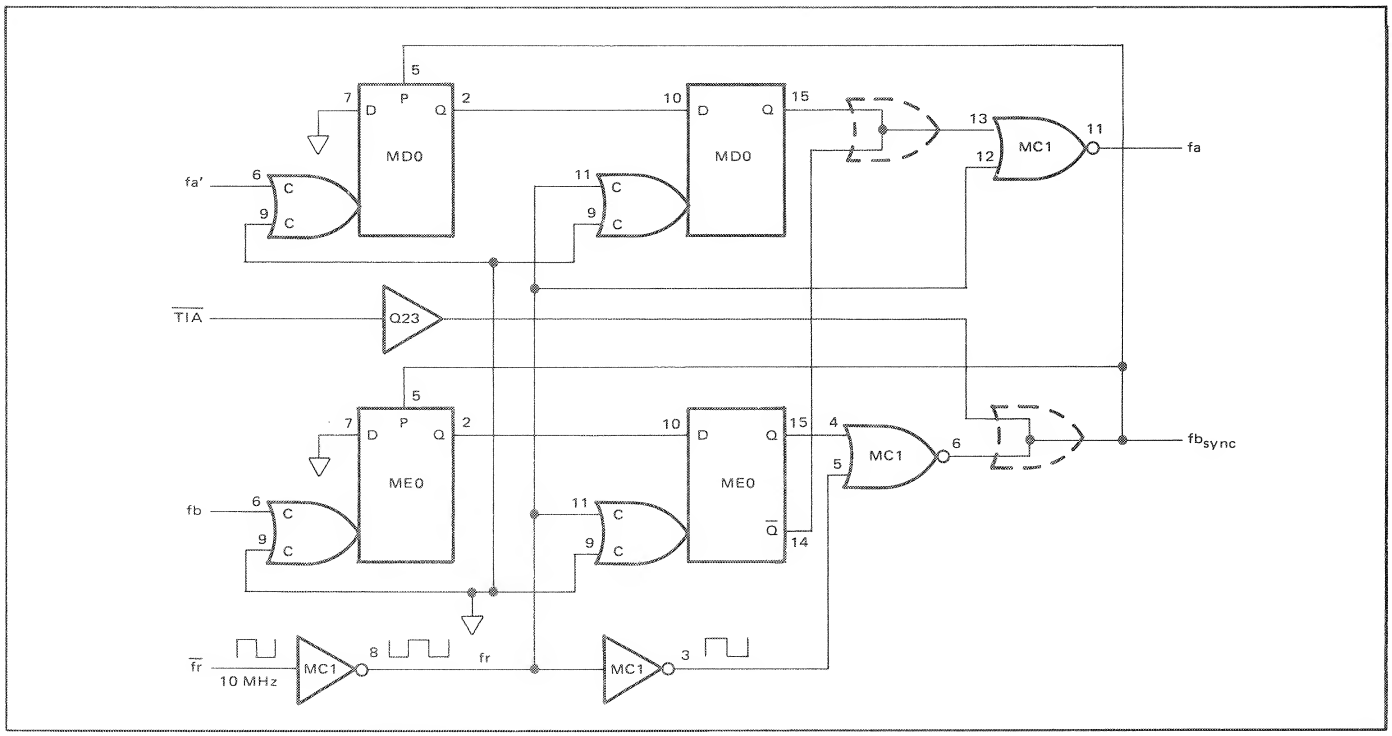


Figure 4.17 - Synchronizer Block Diagram

4.73 SYNCHRONIZER

4.74 The synchronizer circuit is utilized when the Time Interval Average mode is selected. The TIA mode averages a predetermined number of intervals. Two different types of gates are required: a synchronized gate to eliminate the ±1 count error for each interval averaged and a main gate to select the predetermined number of intervals to be averaged. Figure 4.17 shows a block diagram of the synchronizer and the timing diagram is shown in figure 4.18.

4.75 In Time Interval Average mode, the synchronizer will not be enabled until signal f_b SYN pulse occurs.

4.76 The first pulse on channel B (f_b) is routed to the synchronizer and is gated (MC1-6) with the reference signal. The signal f_b SYN, synchronous with the reference signal, is routed to the time base decades. This first f_b SYN pulse causes the time base decades to change from nines to zeros and produces the first f/n pulse. Signal f/n is routed to the START flip-flop in the control logic. The START flip-flop is set by the Start pulse which opens the main gate and generates $\overline{\Delta t}$.

4.77 The synchronizer is now ready to initiate a synchronized gate. The next pulse from channel A is routed to the synchronizer and allows the next reference pulse to open the synchronous gate (MC1-11). The output of the synchronous gate (10^7 counts per second) is routed to the counting decades. Since the main gate is already open because of the previous f_b SYN, the counting decades count the pulses. This is the start of the A-to-B interval measurement.

4.78 The next pulse to arrive on channel B produces f_b. Signal f_b is routed to the synchronizer and allows the next reference pulse to terminate the synchronous gate. The number of f_b SYN pulses to the time base decades required for the second f/n to be generated is dependent on the multiplier setting of the MULTIPLIER/TIMEBASE switches. If the "1" multiplier is selected, f/n is produced with the current f_b SYN pulse. If the "10" multiplier is selected, ten f_b SYN pulses must accumulate in the time base decade before the second f/n is generated. If f/n is not generated before f_a arrives, the pulses from the reference signal do not accumulate in the counter. Signal $\overline{f/n}$ is routed to the STOP flip-flop. The main gate and $\overline{\Delta t}$ are terminated with the second f/n. The display time flip-flop is reset for the display timeout. At the end of the display timeout, the update pulse is generated and the counter decades are reset to zero for a new measurement.

4.79 When the TIA mode is selected, Q23 is turned off releasing the Preset inputs to flip-flops MD0-5 and ME0-5. The output of transistor Q23 and the output of gate MC1-6 form a wired OR gate. The Q outputs of MD0 and ME0 have previously been preset. The Q outputs of MD0-15 and ME0-15 disable gates MC1-13 and MC1-4. Signal f_b

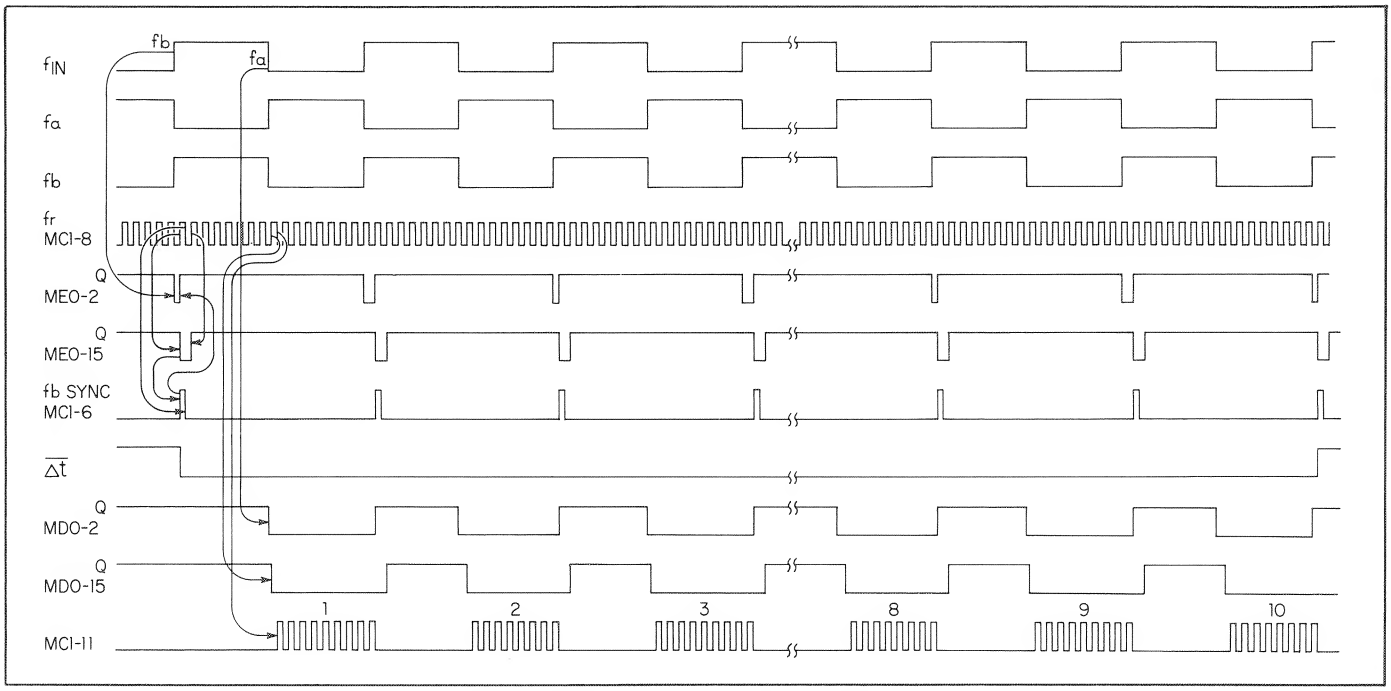


Figure 4.18 - Synchronizer Timing Diagram

clocks the low D input of ME0-7 to the Q output of ME0-2. On the next positive clock (fr) from inverter MC1-8, the low D input on ME0-10 is clocked to the Q output of ME0-15. The low Q output enables gate MC1-4. The reference clock now is inverted and appears at MC1-6. The high output of MC1-6, (f_b SYN) presets the Q outputs of flip-flops MD0-2 and ME0-2 high. Note that the Q output of MD0-2 is high because f_a has not clocked the low D input to the Q output (MD0-2). Signal f_b SYN goes to the multiplier time base decades. The trailing edge of the first f_b SYN causes the outputs of the multiplier time base decades to change state and open the main gate $\overline{\Delta t}$.

4.80 On the next positive clock pulse from inverter MC1-8, the high D input to ME0-10 is clocked to the Q output disabling the gate MC1-6 forming the trailing edge of f_b SYN. The output of gate MC1-6 goes low. The signal f_a arrives at the input to flip-flop MD0 and clocks the low D input to the Q output. The next positive output from inverter MC1-8 clocks the low D input of MD0-10 to the Q output enabling the synchronous gate MC1-11. The reference clock via MC1-8 and MC1-11 flows to the counting decades. Signal f_b arrives at the input to ME0-6 and clocks the low D input to the Q output. The next positive clock pulse from MC1-8 clocks the low D input to the Q output of ME0-15. The Q output of MD0-14 is connected to the Q output of MD0-15 and forms another wired OR gate. $\overline{Q}$ of ME0-14 causes the Q output of MD0-15 to go low disabling MC1-11 and stopping the reference clock to the counting decades. At the same time, gate MC1-6 is enabled for one clock pulse which presets flip-flops MD0-5 and ME0-5, and generates f_b SYN. Signal f_b SYN generates a stop pulse which causes the main gate to close, generation of the update pulse, and a clear to be generated clearing the counting decades. The process begins over again after timeout and the arrival of f_b, then f_a, in that order.

4.81 MULTIPLIER TIME BASE SWITCH LOGIC.

4.82 The interlocking pushbutton switches select one of ten decade divider outputs. The time base decades divide the signal applied to the input by 1, 10, 10^2, 10^3, 10^4, 10^5, 10^6, 10^7, 10^8, or 10^9. The outputs are selectable by the MULTIPLIER/TIME BASE switches. The MULTIPLIER/TIME BASE switch selected pulls the line low. The low level is routed to an inverter through a decoupling diode. The high output is connected to a two-input NAND gate. The other input of the NAND gate is connected to one of the ten outputs of the time base decades. If a multiplier of 10^2 through 10^9 is selected, the output signal of the nand gate is routed through a reclocking circuit. The reclocking circuit is necessary to remove the propogation delays developed in the time base decades. The 1 and 10 multipliers are routed around the reclocking circuit via two nand gates. The output of the gate is the frequency applied to the time base decades divided by the multiplier or f/n.

4.83 Signal f/n is used as a start/stop pulse within the counter and delivered to the rear panel as Scaled Out. Signal f/n is always produced with the first pulse applied to the time base decades and the first pulse is not dependent on the multiplier selected. The time base decades are reset to the nine state at the end of display time when $\overline{T^2\,CLEAR}$ goes low. When the first pulse is applied to the time base

decades, the output of the decades changes from all nines to all zeros. Thus, a change of state of output f/n is produced from any one of the ten multiplier switch positions.

4.84 The signal f/n is derived from various input signals to the time base decades. The reference oscillator (10 MHz) is applied to the input of the time base decades in the Check, Frequency A, Period and Time Interval modes. Selection of the MULTIPLIER/TIME BASE switches determines the repetition rate of f/n. Frequency A is applied to the input in Period Average mode. Selection of the switches determines the number of periods of f_a to be measured before f/n is generated. Frequency B is applied to the input in Ratio and Time Interval Average modes. Selection of the switches selects the number of periods of f_b input to be counted before f/n is generated. Frequency A divided by

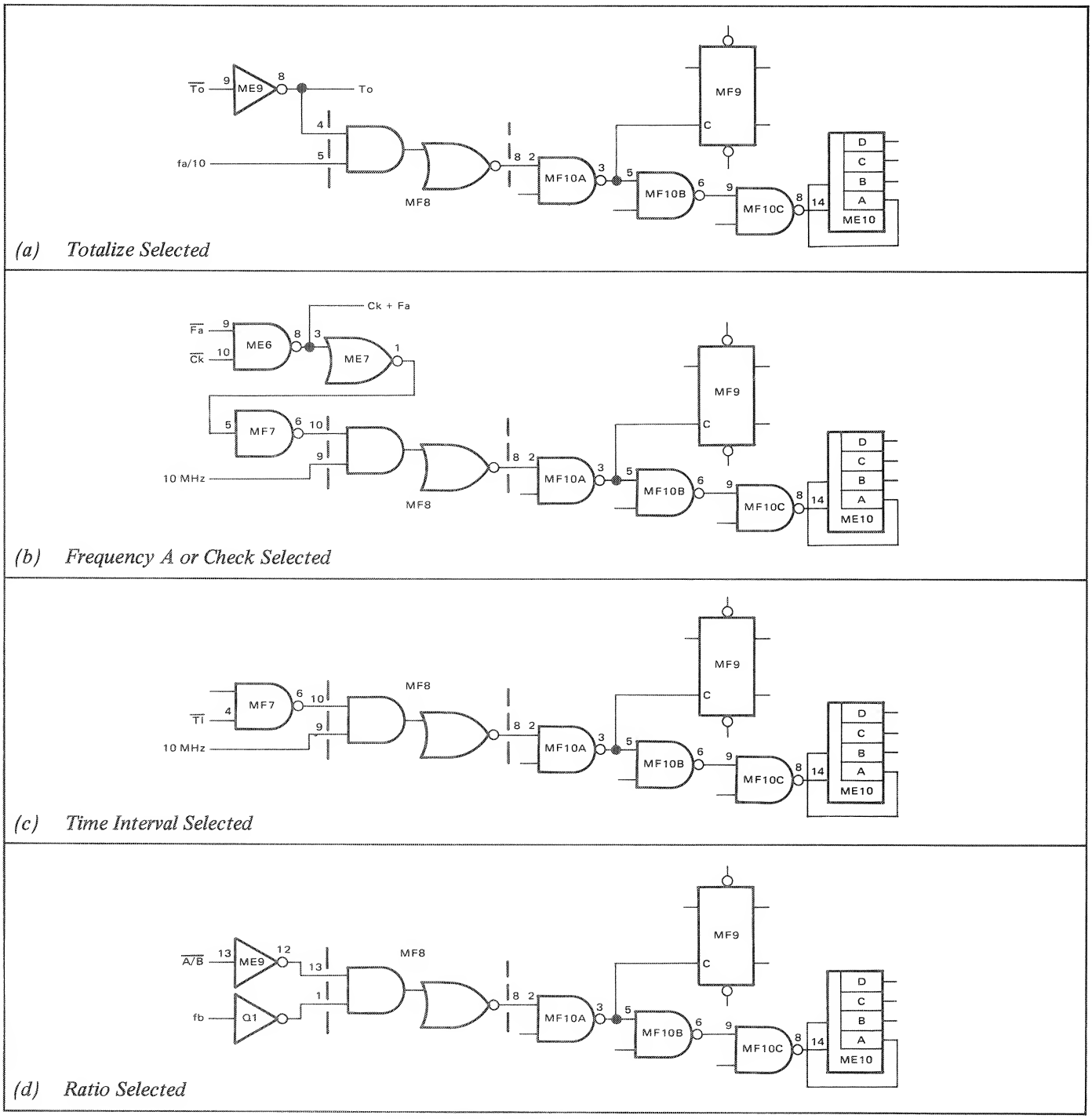


Figure 4.19 - Time Base Steering Logic

continued on page 4-13

ten (f_a/10) is applied to the input in the Totalize mode. Selection of the switches determines the scaling factor of f/n. The reference oscillator divided by four is applied to the time base decades in the Frequency C mode. Selection of the switches determines the repetition rate of f/n. Signal f/n is used for the start/stop pulses which establish the gate time.

4.85 TIME BASE STEERING LOGIC.

4.86 This circuitry routes signals to the time base divider circuit according to the measurement mode selected. Signal flow through the circuit is shown in figure 4.19a through h.

4.87 Totalize Mode.

4.88 Signal flow through the Time Base Steering logic in the Totalize Mode (figure 4.19a) is as follows. The Totalize mode is selected by the FUNCTION switch and $\overline{TO}$ is pulled to ground. $\overline{TO}$ is connected through inverter ME9 to an expandable 4-wide 2-input Nor gate, MF8. The output of MF8 is routed through Nand gates MF10A, and MF10C. The output of MF10C is applied to the clock input to the time base decades (MF9-14).

4.89 Frequency A or Check Mode.

4.90 Signal flow through the Time Base Steering logic in the Frequency A or Check mode is as follows (figure 4.19b). Frequency A or Check mode is selected by the FUNCTION switch which pulls one of the two lines $\overline{FA}$ or $\overline{Ck}$ to ground. These two lines are connected to Nand gate ME6. The output of ME6 (Ck + Fa) is connected to Nor gate ME7. The signal (Ck + Fa) is inverted through ME7. The output of ME7 is applied to Nand gate MF7. The output of MF7 is tied to pin 10 of a expandable 4-wide 2-input Nor gate MF8. The input of MF8 is high, thus enabling gate MF8. The 10 MHz reference, connected to pin 9 of MF8, passes on through MF10A, MF10B, MF10C, to the time base decades.

4.91 Time Interval Mode (Not in Model 8020B).

4.92 Signal flow through the Time Base Steering logic in the Time Interval mode is as follows (figure 4.19c). Time Interval is selected by the FUNCTION switch which pulls the TI line to ground. The $\overline{TI}$ line is connected to the input to Nand gate MF7. The other input, being high, causes the output of MF7 to be high. The output of MF7 is connected to one of two inputs to Nand gate MF8. The other input to MF8 is the 10 MHz reference. Since this gate is enabled, the 10 MHz reference passes through to MF10A, MF10B, MF10C, and to the time base decades.

4.93 Ratio Mode (Not in Model 8020B).

4.94 The signal flow through the Time Base Steering logic in Ratio mode is as follows (figure 4.19d). Ratio (A/B) is selected by the FUNCTION switch. The switch pulls the A/B line down to ground. The $\overline{A/B}$ line is routed to Inverter ME9. The output of ME9 is applied to pin 13 of MF8. The other input (pin 1) is tied to transistor Q1. When Q1 is on, pin 1 of MF8 is high and gate MF8 is enabled. The signal, f_b, passes through MF8 to MF10A, MF10B, and MF10C to the time base decades.

4.95 Time Interval Average Mode.

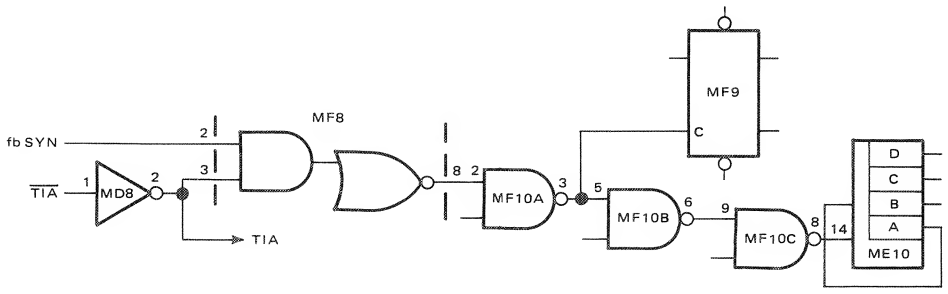
4.96 The signal flow through the Time Base Steering logic in the Time Interval Average mode is as follows (figure 4.19e). The Time Interval Average mode is selected by the FUNCTION switch which pulls the $\overline{TIA}$ line down to ground, the $\overline{TIA}$ line is connected to Inverter MD8. The output of MD8, is connected to pin 3 of MF8. The other input of MF8 pin 2 is connected to f_b SYN. With gate MF8 enabled, f_b SYN signal passes through MF8 to MF10A, MF10B, and MF10C to the time base decades.

4.97 Period Average Mode.

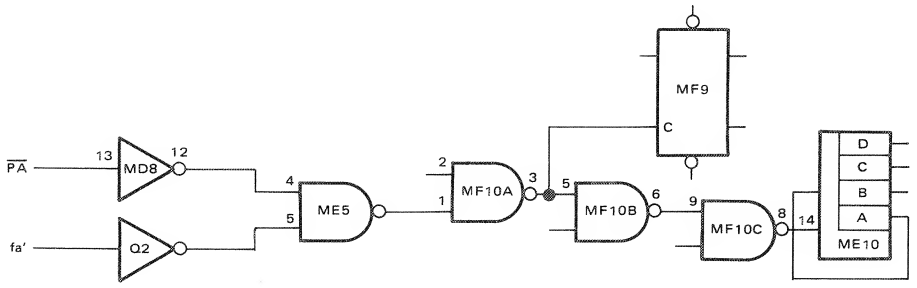
4.98 The signal flow for the Time Base Steering in Period Average mode is as follows (figure 4.19f). The Period Average mode is selected by the FUNCTION switch, which pulls the $\overline{PA}$ line low at the input of inverter MD8. The output of MD8 is connected to one input of Nand gate ME5. The other input of ME5 is connected to fa'. Signal fa' passes through ME5 to MF10A. Nand gate MF10A is enabled and fa' is applied to MF10B and MF10C, to the time base decades.

4.99 Frequency C and Period Modes.

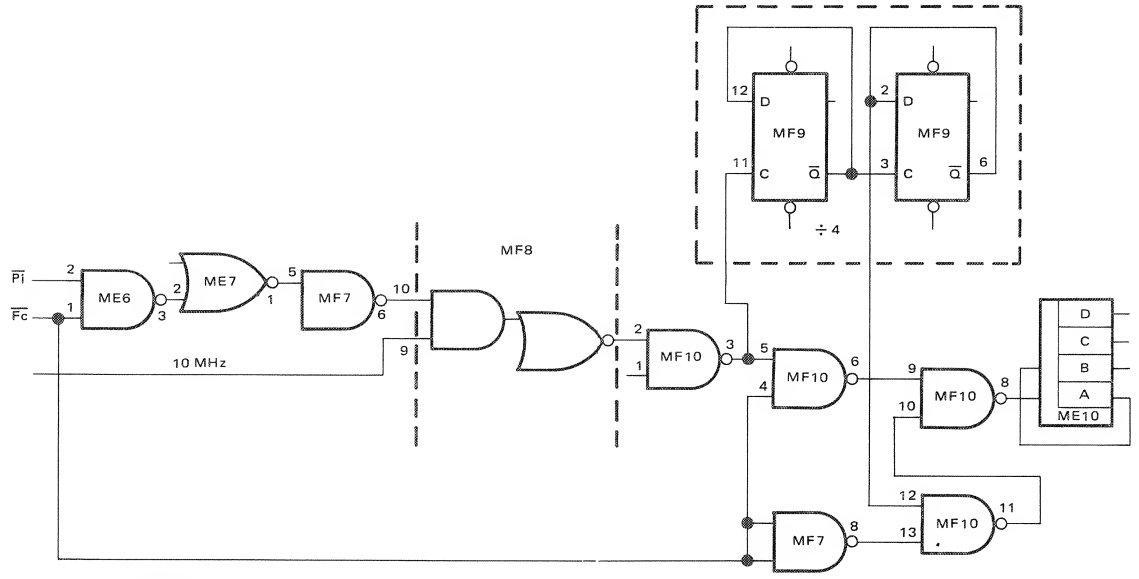
4.100 The signal flow for the Time Base Steering in Frequency C and Period modes is as follows (figure 4.19h). Frequency C or Period is selected by the FUNCTION switch. The FUNCTION switch pulls one of the two control lines, $\overline{Fc}$ or $\overline{Pi}$, low. Both lines are connected to Nand gate ME6. The output of ME6 is high and is connected to Nor gate ME7. The output of ME7 is connected to Nand gate MF7 and is low. The output of MF7 is connected to pin 10 of MF8 and is high. This enables the 10 MHz reference to pass through MF8 to Nand gate MF10A. The signal flow in the Period mode is from MF10A to MF10B, to MF10C, to the time base decades. The signal flow in Frequency C mode is from MF10A to a type D flip-flop, MF9, connected as a divide-by-four counter. The output of MF9 is applied through Nand gate MF10D to MF10C and to the time base decades.



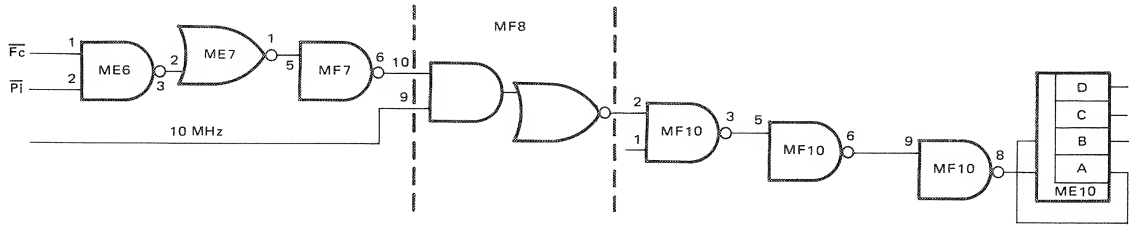
(e) Time Interval Average Selected



(f) Period Average Selected



(g) Frequency C Selected



(h) Period Selected

Figure 4.19 - Time Base Steering Logic

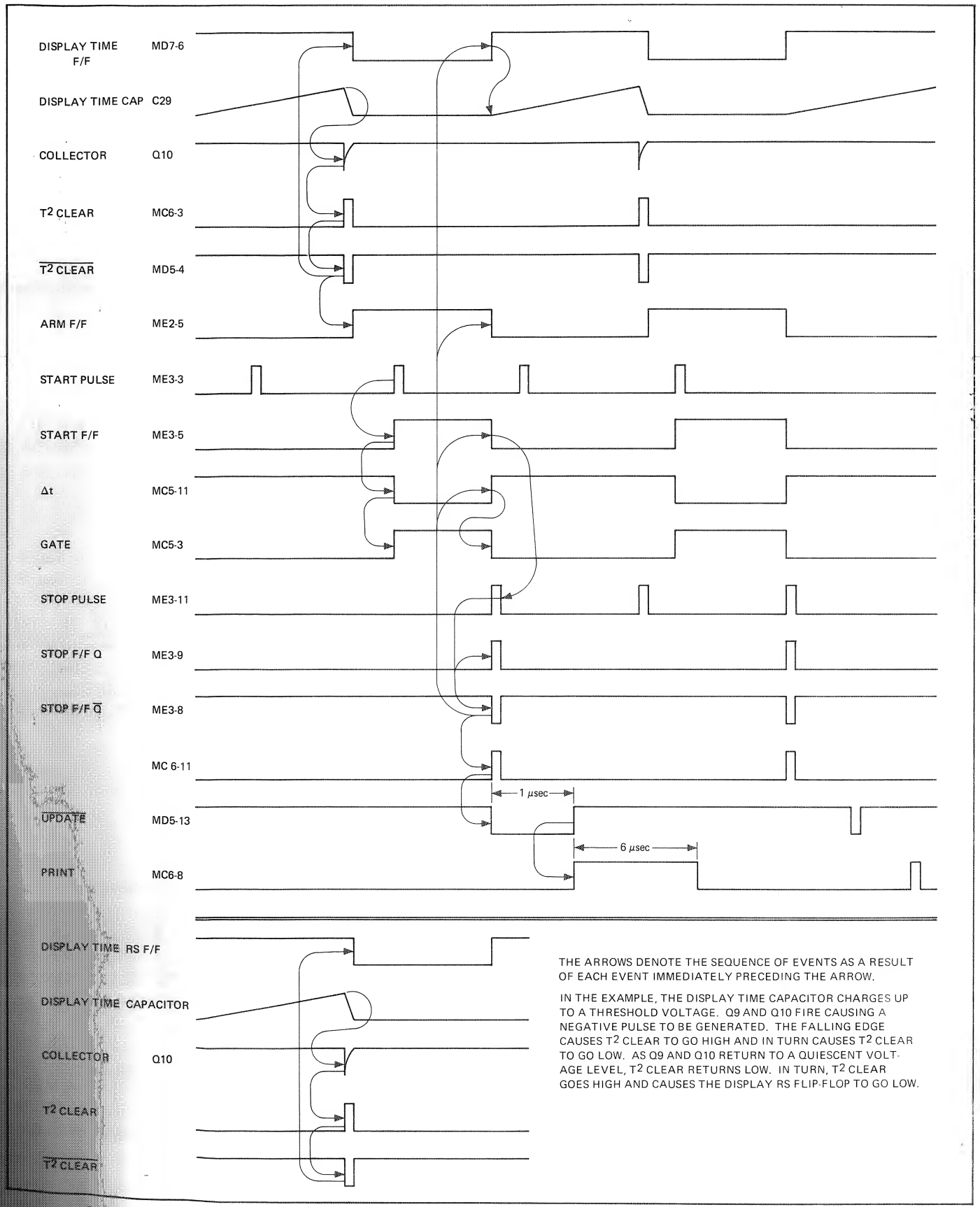


Figure 4.20 - Control Logic Timing

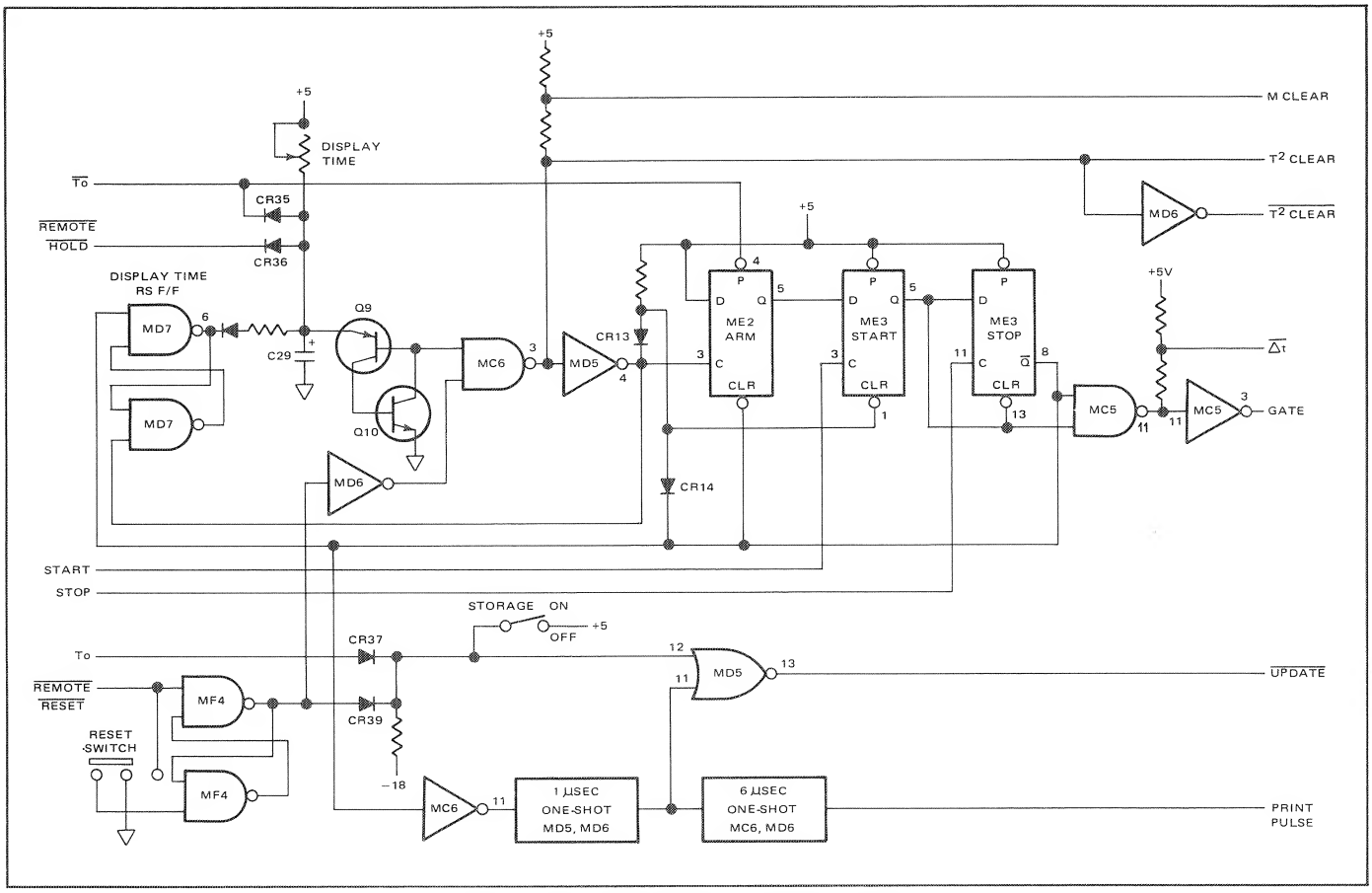


Figure 4.21 - Block Diagram Control Logic

4.101 CONTROL LOGIC.

4.102 This circuitry controls the timing sequence for the balance of the instrument; it generates the main gate control signal ($\overline{\Delta t}$). The timing sequence is illustrated in the timing diagram of figure 4.20, the circuitry is shown simplified in figure 4.21. With the DISPLAY TIME control set to produce periodic readings (not in the HOLD position), the operating sequence for all modes, except Totalize, begins when MD7-6 goes high. The display time integrating capacitor C29 charges at a rate dependent on the setting of the DISPLAY TIME control. When the voltage across C29 reaches approximately +3.7 volts, a latching circuit (Q9 and Q10) fires. Gate output MC6-3 goes high and inverter output MD5-4 goes low, resetting the display time RS flip-flop MD7. The voltage across C29 is discharged, Q9 and Q10 is reset, and MC6-3 goes low. From the previous reading, ME2-5 is low, ME3-5 is low and ME3-8 is high. An inverted T^2 CLEAR pulse (MC6-3), generated by the display time circuit, is fed to the clock input of a type D flip-flop ME2-3 and sets ARM (ME2-5) high on the trailing edge of the pulse. The instrument is now ready to measure. A START pulse to ME3-3 (clock) sets the Q output (ME3-5) high, causing $\overline{\Delta t}$ to go low (MC5-11) and MAIN GATE (MC5-3) to go high and enables STOP flip-flop so it will respond to the next STOP pulse.

4.103 When a STOP pulse is received at ME3-11 (clock), ME3-8 goes low causing $\overline{\Delta t}$ to go high and MAIN GATE to go low. The same ME3-8 signal is inverted and fires the 1-microsecond one-shot (MD5, MD6). The output of the one-shot is inverted through MD5 to produce the $\overline{\text{UPDATE}}$ pulse. At the same time, ME3-5 is reset low (through CR14 to ME3-1) which causes ME3-8 to reset high (through ME3-13). At the completion of the 1-microsecond one-shot, a 6-microsecond one-shot (MC6, MD6) fires. The output is inverted by MC6 to form the PRINT pulse used with Systems Interface, Option 008.

4.104 In the Totalize mode, the operation of the circuitry is the same with the following exceptions: the selection of Totalize sets MD5-12 true through CR37, causing MD5-13 to go false ($\overline{\text{UPDATE}}$). This allows the accumulation of pulses in the counter to be continuously monitored by the operator. Also, pin 4 of ME2 is held to ground, presetting Pin 5 of ME2 (ARM) to high and the display time circuit is disabled through CR35. The Start/Stop pulses are generated manually by the START/STOP switch on the front panel or

electrically through the external gate line (EXT. GATE) and perform the same function as the internally generated pulses in the other measurement modes. However, since the ARM line is held high as long as the instrument is in the Totalize mode, the Totalize measurement may be started and stopped as many times as desired.

4.105 The reset circuit (MF4) is used to reset the Counting Decades. In REMOTE HOLD, for modes other than Totalize, the reset commands a new reading.

4.106 START/STOP LOGIC.

4.107 The Start/Stop logic generates the Start and Stop pulses used by the control logic to control the main gate. The Start pulse is used to set the Start flip-flop (in the control logic) which initiates the gate. The Stop pulse sets the Stop flip-flop. The output of the Stop flip-flop terminates the gate. The routing of the signals is shown in figure 4.22a through e.

4.108 Totalize Mode (figure 4.22a).

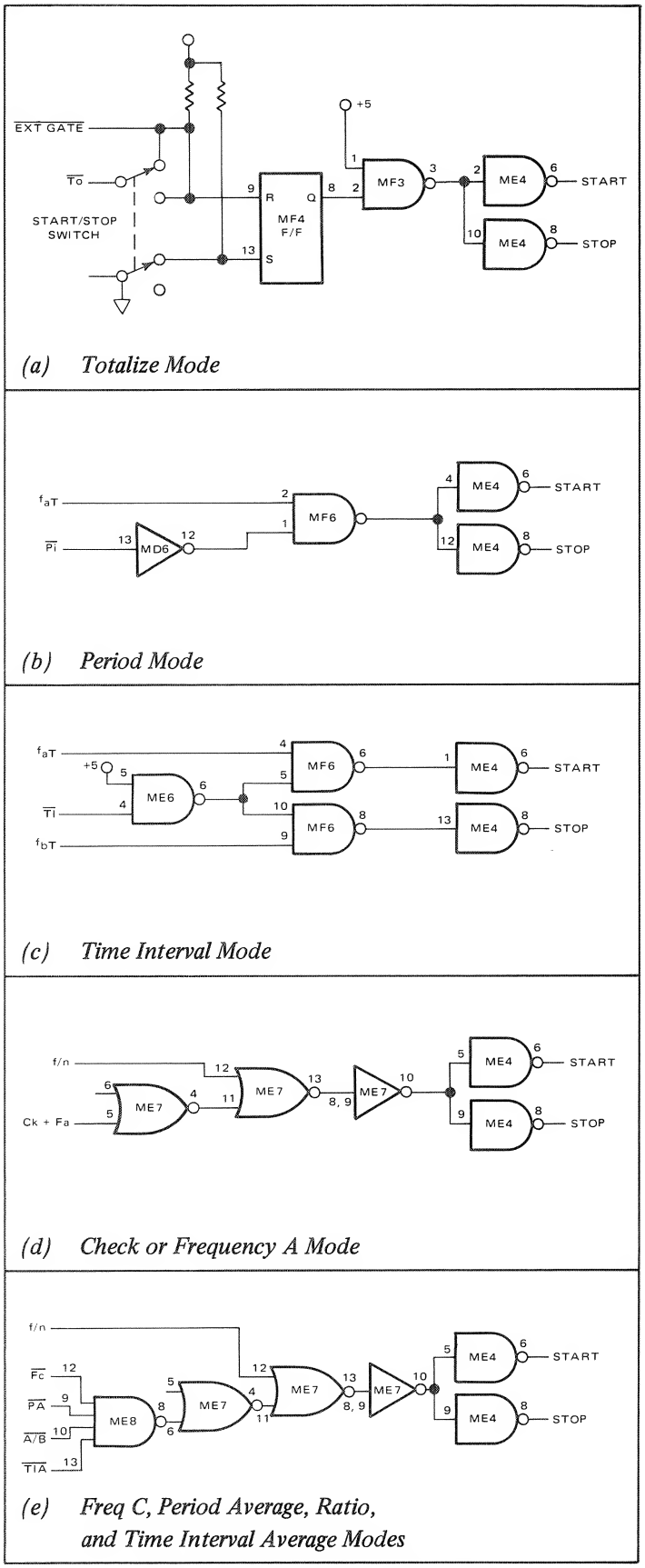
4.109 In the Totalize mode the start pulse is initiated by the START/STOP switch or by the external gate line pulled to common. The START/STOP switch and the external gate lines are tied to the input of an RS flip-flop (MF4) made from two cross-coupled nand gates. The output of the flip-flop is low when the START/STOP switch is not depressed. When the switch is depressed, the inhibit is removed and the flip-flop output goes high. The output stays high as long as the switch is depressed or the external gate line is pulled to common. The output of the flip-flop is tied to inverter MF3. The output of the inverter is connected to two four-input nand gates. The gate is initiated on the first Start/Stop command and terminated on the second.

4.110 Period Mode (figure 4.22b).

4.111 In the Period mode, the $\overline{Pi}$ line is low causing the output of inverter MD6 to enable nand gate MF6. The rising edges of f_{aT} (frequency A at TTL level), produces Start and Stop pulses for the control logic.

4.112 Time Interval Mode (figure 4.22c).

4.113 In the Time Interval mode, the $\overline{TI}$ line is low. $\overline{TI}$ is inverted through ME6-6 which enables Nand gates MF6-6 and MF6-8. When Frequency A triggers and f_{aT} rises, it causes the output of MF6-6 to go low. This causes a Start to be generated at the output of ME4. When Frequency B triggers and f_{bT} rises, it causes the output of MF6-8 to go low. This causes a Stop to be generated at the output of ME4-8.



(a) *Totalize Mode*

(b) *Period Mode*

(c) *Time Interval Mode*

(d) *Check or Frequency A Mode*

(e) *Freq C, Period Average, Ratio, and Time Interval Average Modes*

Figure 4.22 - Start/Stop Signal Flow

4.114 Check or Frequency A Mode (figure 4.22d).

4.115 In the Check or Frequency A mode, Ck + Fa is high and is connected to Nor gate ME7-5. The other input to ME7-6 is low. The output of ME7-4 is low and is connected to Nor gate ME7-11. The other input to ME7-12 is connected to the scaled output (f/n). The scaled output is the reference oscillator frequency divided by the time base decade selection.

4.116 Frequency C, Period Average, Ratio, and Time Interval Average Modes (figure 4.22e).

4.117 In the Frequency C, Period Average, Ratio, and Time Interval Average modes, one of the inputs ($\overline{Fc}$, $\overline{PA}$, $\overline{A/B}$, $\overline{TIA}$) to Nand gate ME8 is selected and pulled low. The output of ME8-8 goes high and Nor gate ME7-4 goes low enabling Nor gate ME7-13. The gate is initiated when f/n goes low via the Start pulse at ME4-6. The next time f/n goes low the gate is terminated via the Stop pulse at ME4-8.

4.118 MARKER LOGIC (figure 4.23).

4.119 The MARKER output provides a negative 18-volt pulse starting when channel A triggers and stopping when B triggers. It is used for increasing the intensity of an oscilloscope trace.

4.120 The circuit consists of two D-type flip-flops (ME1) driving a voltage level shift circuit (Q16, Q17). Channel A input (f_{aT}) sets ME1-6 low causing Q16 to turn off. In turn, Q17 turns off producing a −18 volt output at the collector of Q17. A trigger from the channel B input (f_{bT}) sets the second half of ME1. Q resets ME1-6 high causing transistors Q16 and Q17 to saturate and producing a collector output of about zero volts for the marker output at J103.

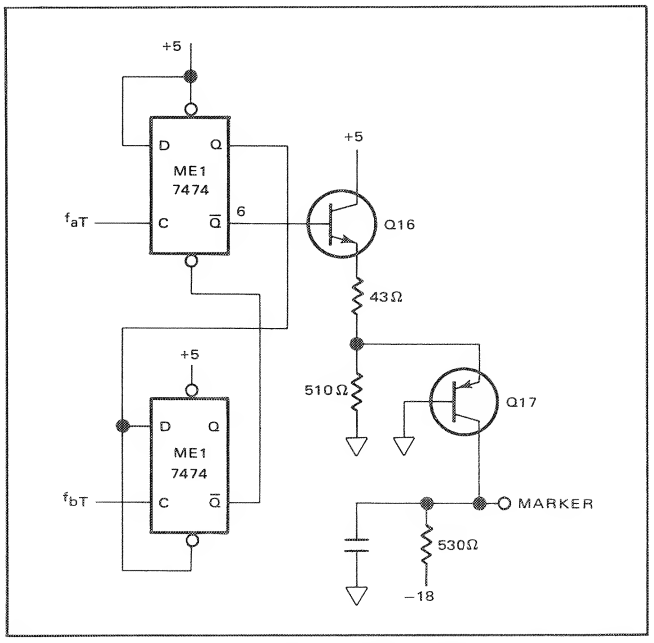


Figure 4.23 - Marker Logic

4.121 Readout Board.

4.122 The readout board assembly is one of two large printed circuit boards mounted to the base plate. The readout board is accessible from the top of the counter. The readout board contains the following circuits; the reference oscillator, the power supply, the function switch, the display tubes, the TTL counting decades, and the storage.

4.123 COUNTER/DISPLAY.

4.124 The counter and display circuit counts, stores and displays the number of pulses received from the high-speed decade on the switch board. The counter consists of seven decade counters (type 7490), eight quadruple bistable latches (type 7475), eight numeric display tube drivers (type 7441), and eight numeric display tubes. An additional tube, driver, latch, and decade are included in instruments having the 9th digit, Option 004. Transistor Q1 controls the update inputs of all the quad latches. A low update signal from the control logic allows each latch to assume the same level as the decade counter to which it is connected. A high update signal allows the latches to store the information. The T^2 CLEAR line (when low) resets the decade counters to zero.

4.125 POWER SUPPLY.

4.126 The power supply (figure 4.24) provides all voltage levels for the operation of the instruments and standby power (with power OFF selected) for the continuous operation of the optional frequency source (with instruments equipped with Option 200). All supplies except the +150 volt supply are regulated.

4.127 The +150V supply is used by the gas tube display and derived from a +250 volt full wave bridge circuit. Current limiting resistor R60 drops the voltage to the tubes to approximately +150 volts when the tubes are conducting. With power OFF, the +150 line is opened.

4.128 The +28 volt supply is used only for the optional frequency reference (Option 200) and is derived from a tapped secondary full wave rectified circuit and discrete 28-volt regulator.

4.129 The −18-volt supply is used throughout the instrument and is derived from a −28 volt full wave rectified supply and a regulator consisting of zener CR20 and transistors Q26 and Q101. Referring to the schematic, Q26 and

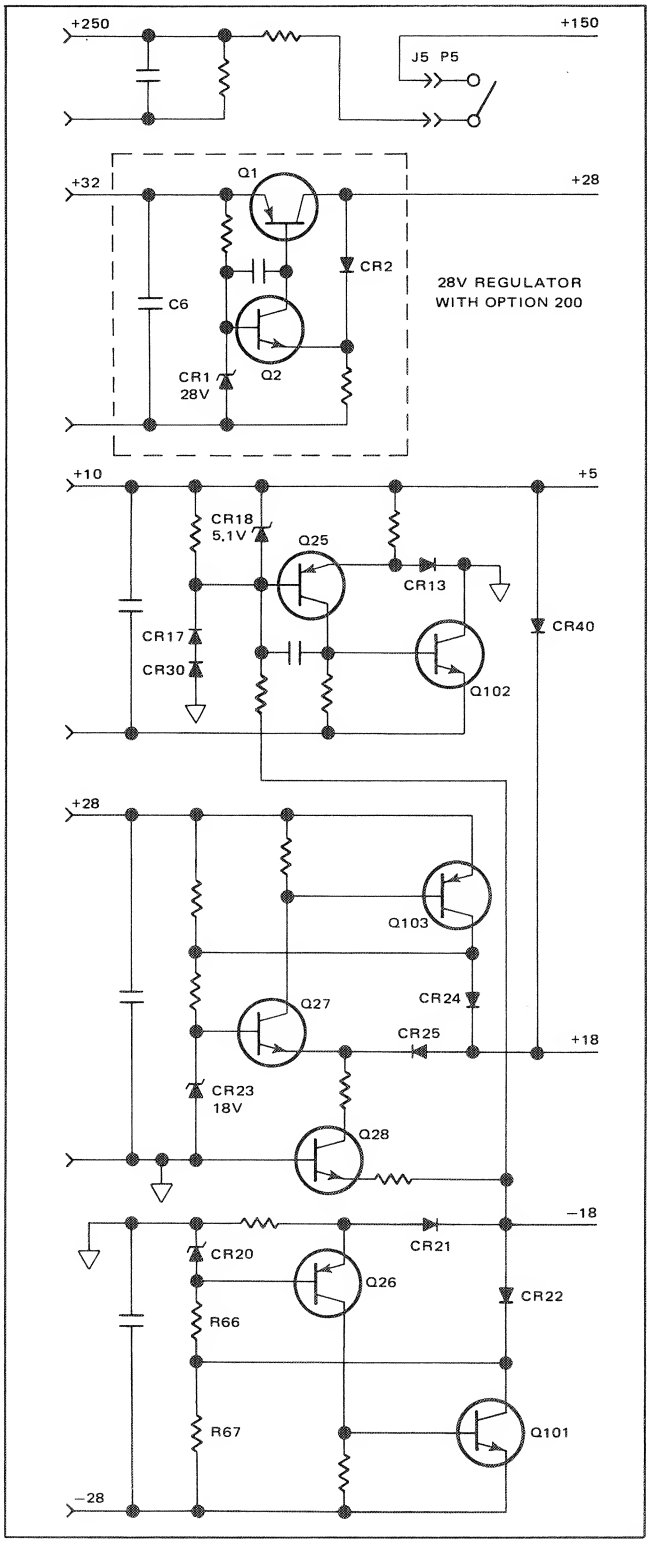


Figure 4.24 - Power Supply

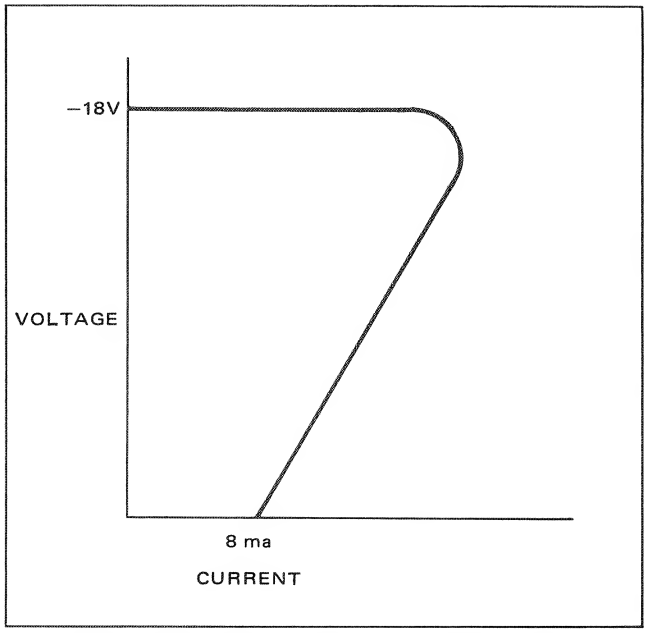


Figure 4.25 - Characteristic of -18V Regulator

CR20 (18 volt zener) form a 12 milliamp current generator with resistors R66 and R67 supplying current to the zener. The base of Q101 is driven by the current generator causing Q101 to conduct heavily pulling the output towards -28 volts through diode CR22. At -18 volts, diode CR21 starts conducting causing the current generator to lessen the output and at this point stability is reached. When the power switch is set to OFF the -18 volt supply is shorted to ground. The voltage at the cathode of CR22 turns off Q26 by depriving CR20 of idling current and the short circuit current folds back to approximately 8 ma as shown in figure 4.25.

4.130 The +18 volt supply is also used throughout the instrument and is derived from a +28 full wave rectified circuit. The regulator circuit, consisting of transistors Q27, Q28, Q103, and 18 volt zener CR23, operates in the same manner as the -18 volt supply. Transistor Q28 functions as a switch and turns off the +18 supply when the -18 volt supply goes to ground (instrument is shut off).

4.131 The +5 volt supply is used by all of the digital circuitry. The regulator operates in the same manner as the ±18 volt supplies but uses a 5-volt zener. The current for the zener is supplied through resistor R63 from the -18 volt supply.